U/S...
EQUALIZATION

CU SENDS MESSAGE TO RU TELLING IT TO SEND EQUALIZATION DATA TO CU USING ALL 8 OF THE FIRST 8 ORTHOGONAL CYCLIC CODES AND BPSK MODULATION.

1116

RU SENDS SAME TRAINING DATA TO CU ON 8 DIFFERENT CHANNELS SPREAD BY EACH OF FIRST 8 ORTHOGONAL CYCLIC CODES.

1118

CU RECEIVER RECEIVES DATA, AND FFE 765, DFE 820 AND LMS 830 PERFORM ONE INTERATION OF TAP WEIGHT(COEFFICIENT) ADJUSTMENTS.

1120

TAP WEIGHT (COEFFICIENT) ADJUSTMENTS CONTINUE UNTIL CONVERGENCE WHEN ERROR SIGNALS DROP OFF TO NEAR ZERO.

1122

AFTER CONVERGENCE DURING TRAINING INTERVAL, CU SENDS FINAL FFE AND DFE COEFFICIENTS TO RU.

IN CU

1124

~~RU~~ ~~SETS~~ CONVOLVES FINAL FFE & DFE SE CIRCUIT COEFFICIENTS ~~INTO~~ WITH OLD PRECODE FFE/DFE FILTER IN TRANSMITTER COEFFICIENTS AND LOAD NEWLY CALCULATED COEFFICIENTS INTO RU XMTR PRECODE FILTER

RU

TRANSPARENCY VALUES

1126

CU SETS COEFFICIENTS OF FFE 765 AND DFE 820 TO ~~ONE~~ TRANSPARENCY VALUES FOR RECEPTION OF UPSTREAM PAYLOAD DATA.

TO FIG. 45C

~~54B~~
FIG. ~~45B~~
53B

FAXED TO
DI MUELLER
10/25/00
(909) 596-3733

DOWNSTREAM EQUALIZATION

FROM FIG. 45B

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

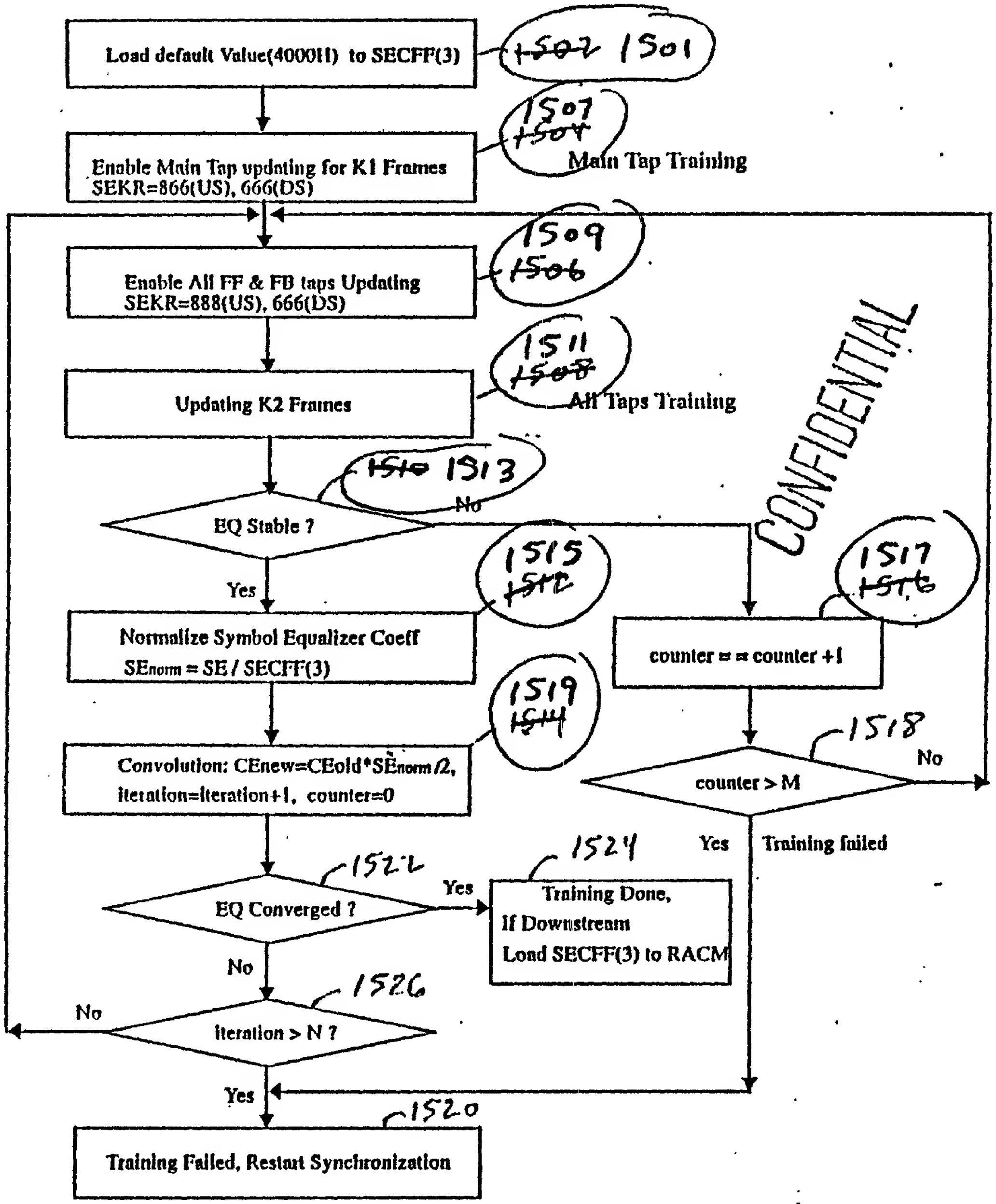
1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND ~~LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764~~; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

CONVOLVES THESE SE FILTER TAP WEIGHTS WITH THE OLD FILTER TAP WEIGHTS OF THE FFE AN[D] DFE FILTERS O[F] CE CIRCUIT 764 AND LOADS THE NEWLY CALCULA[T]ED TAP WEIGHT[S] INTO THE FFE AND DFE FILTERS OF THE CE CIRCU[IT]

FIG. ~~45C~~ ~~54C~~ 53C

Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING
FIG. 60

Sent to A2 July 97

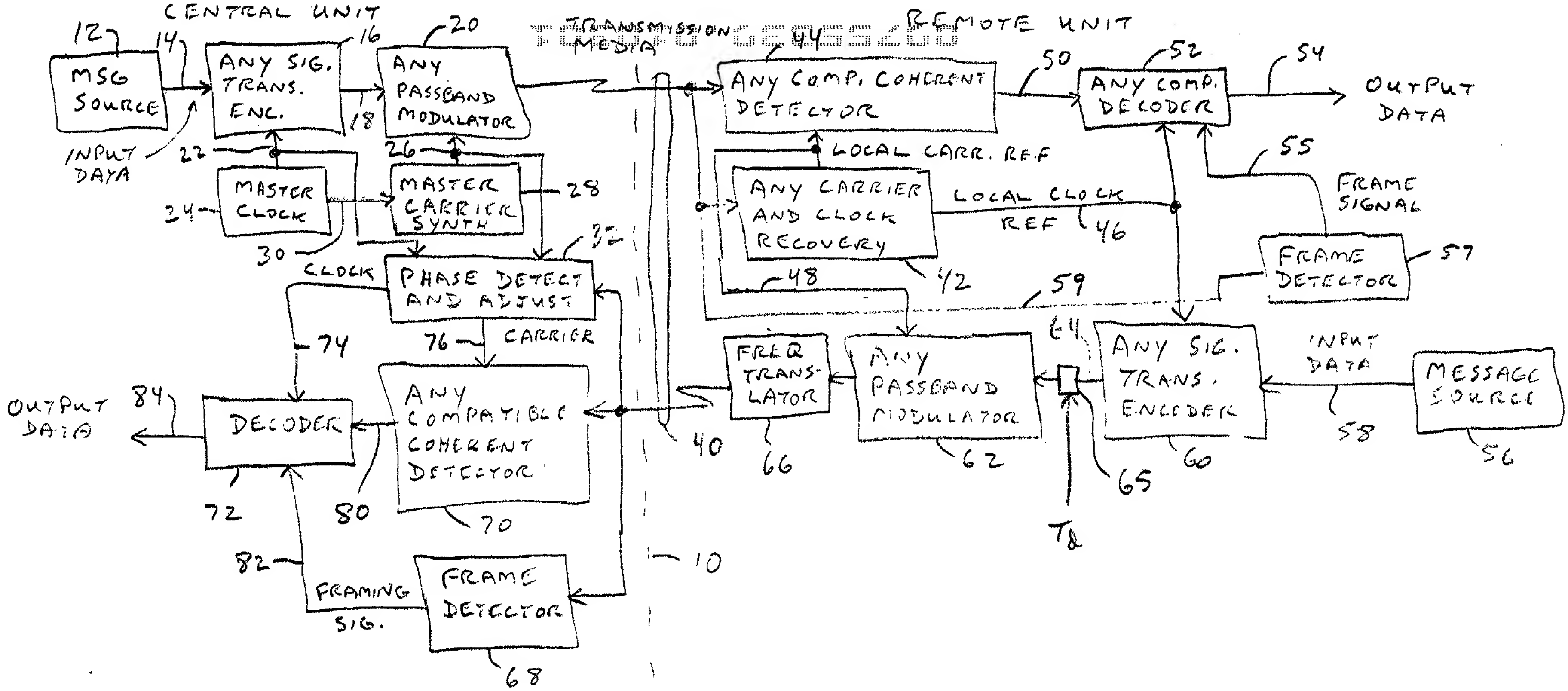


FIG. 1

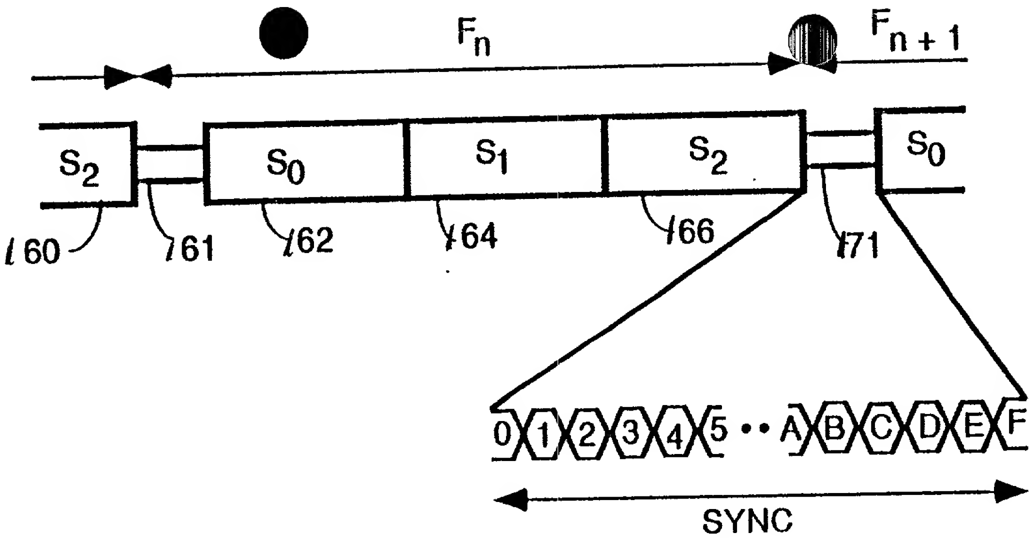


FIG. ~~4A~~ 2A

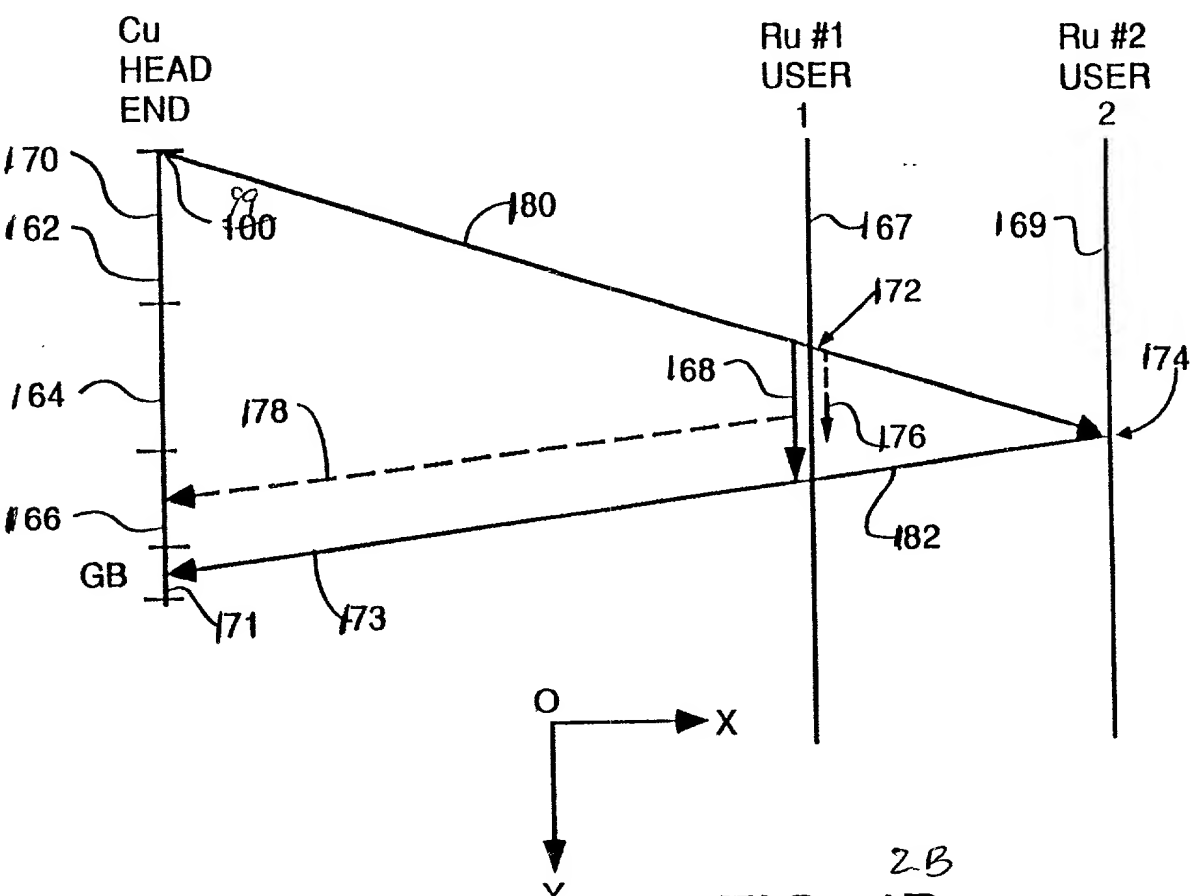


FIG. ~~4B~~ 2B

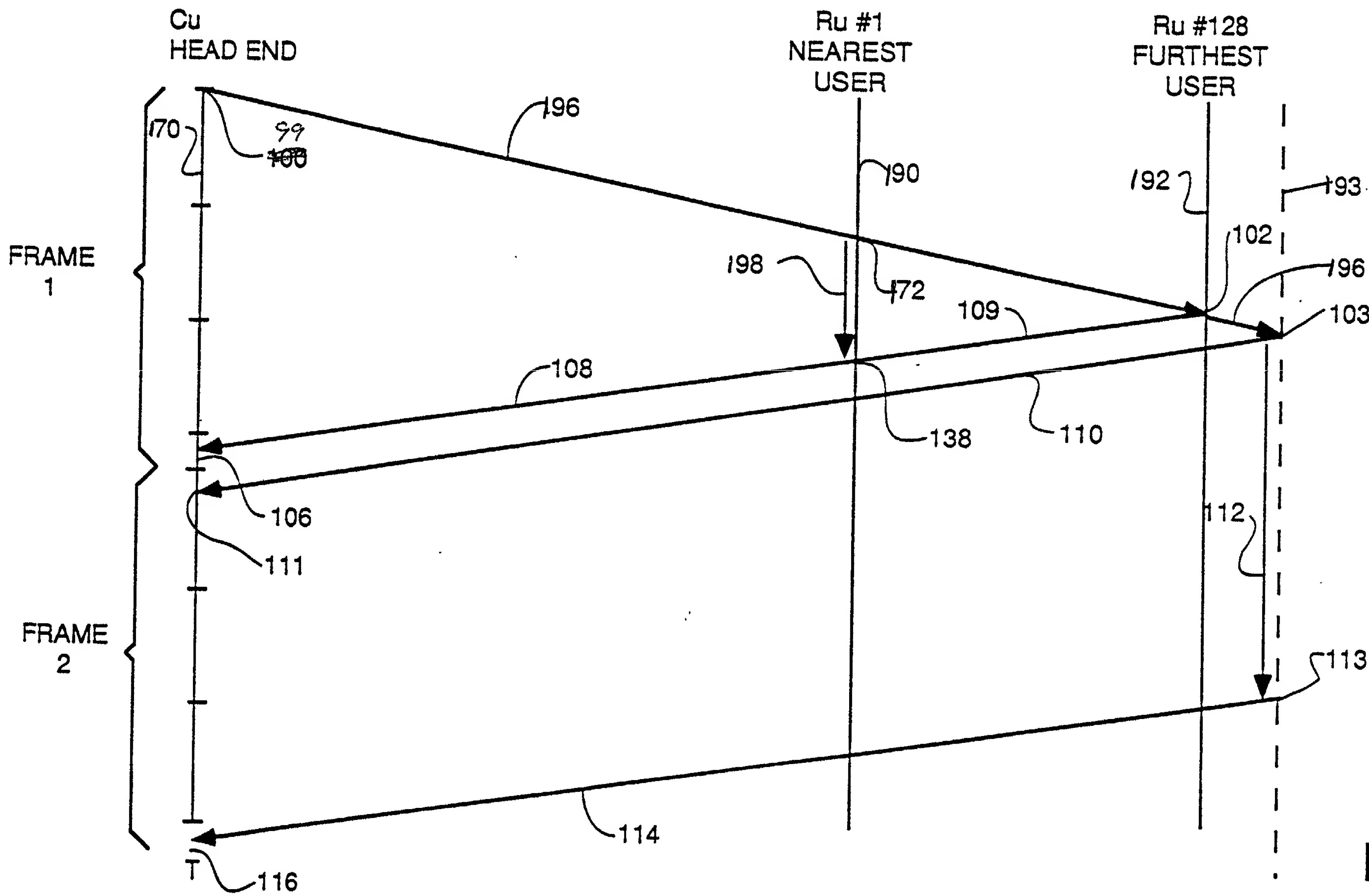

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
FRAME
1
FRAME
2
196
170
99
~~100~~
190
192
193
102
196
198
172
109
103
108
138
110
106
111
112
113
114
116
T

FIG. ~~5~~ 3

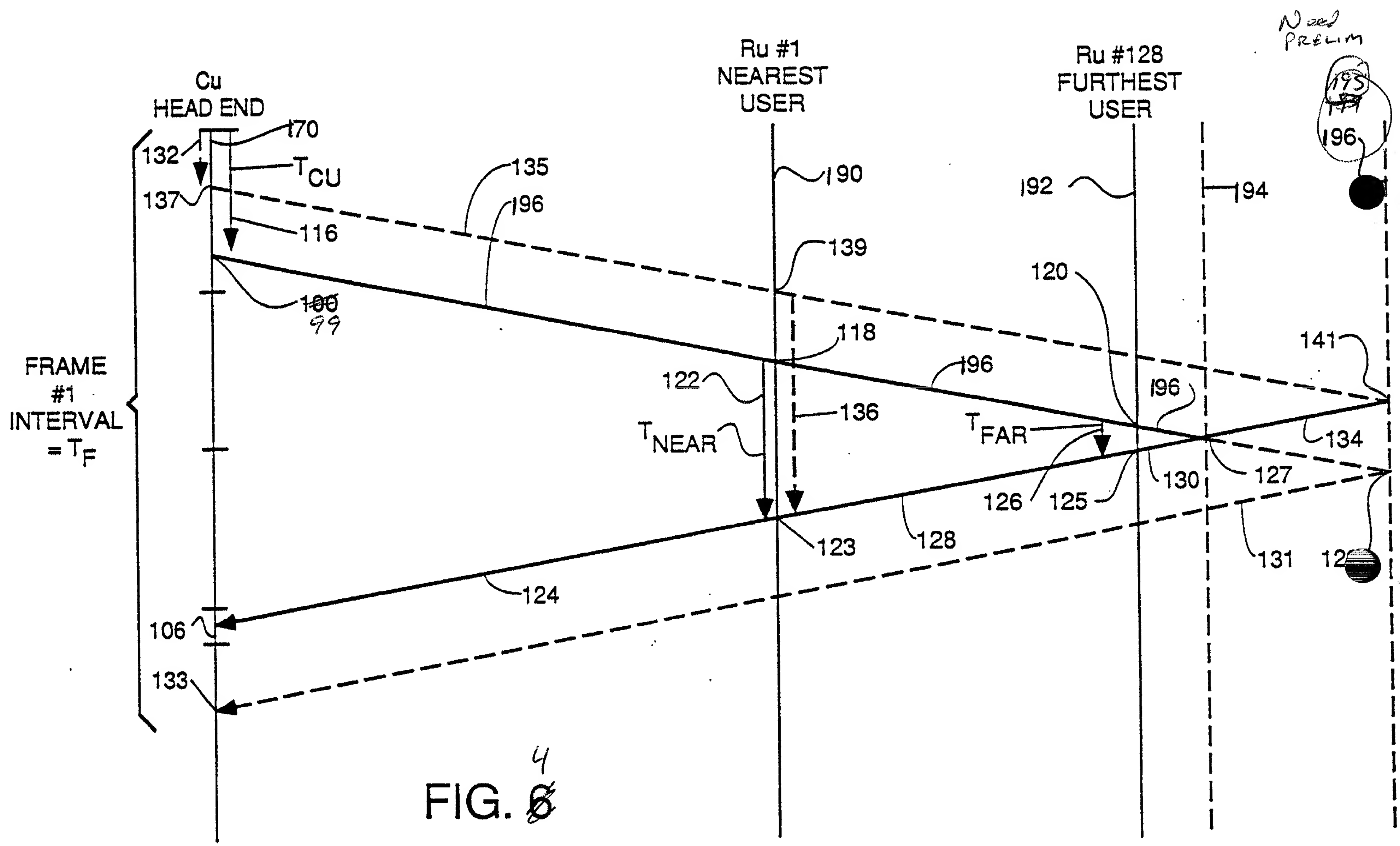
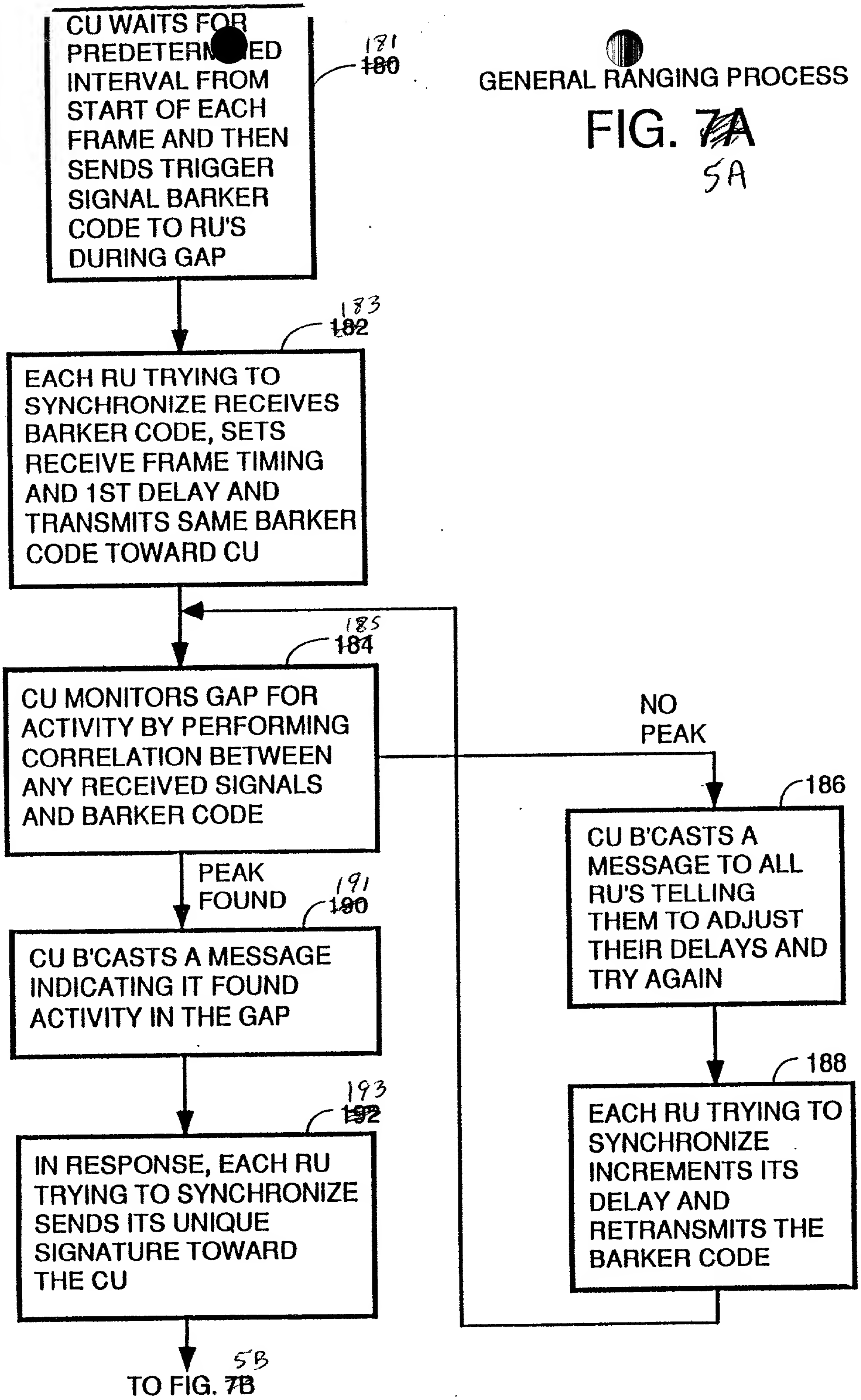
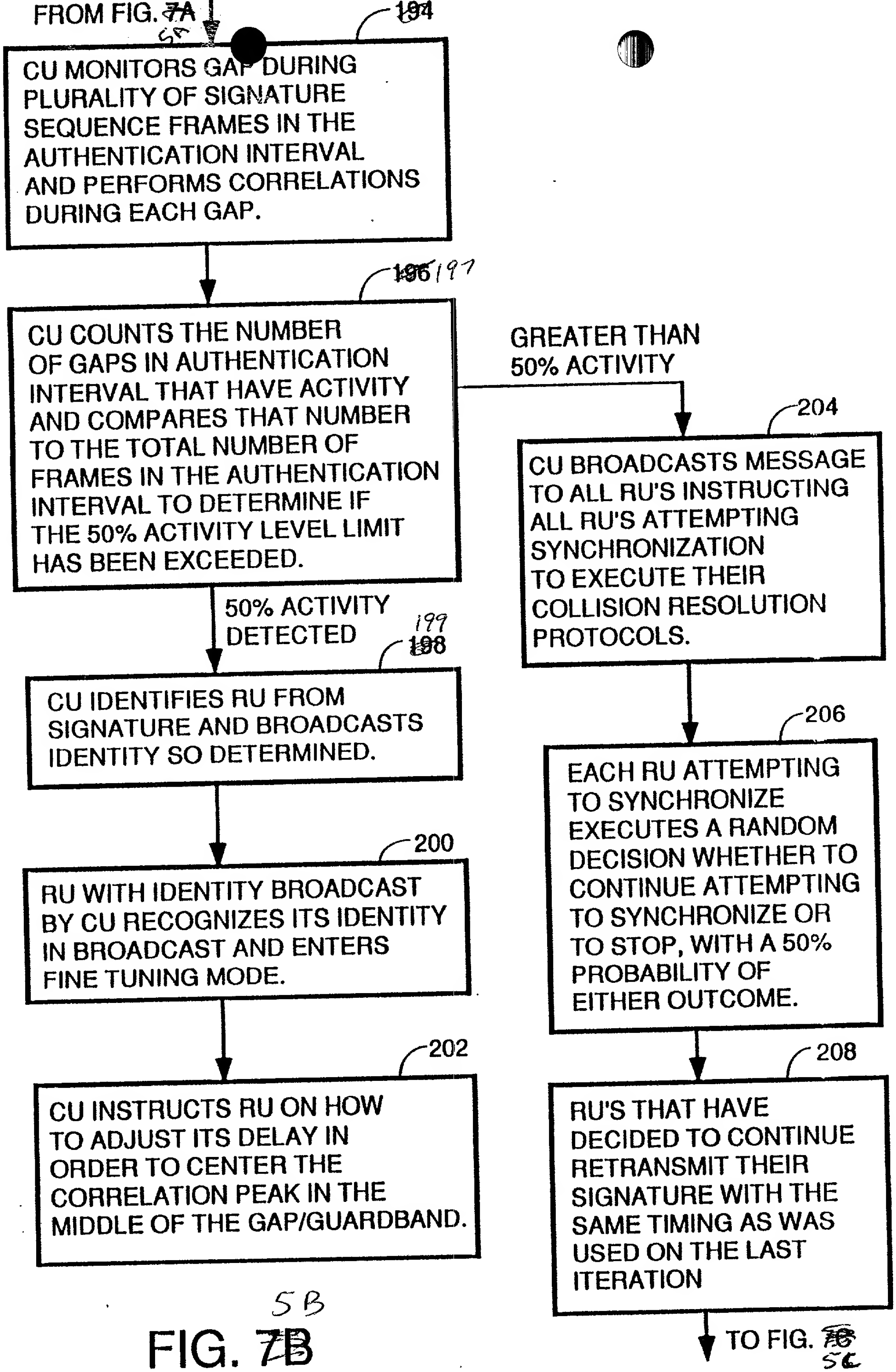

Cu
HEAD END
Ru #1
NEAREST
USER
Ru #128
FURTHEST
USER
Need
PRELIM
FRAME
#1
INTERVAL
= T_F
T_{CU}
T_{NEAR}
T_{FAR}
170
132
137
116
135
196
~~100~~ 99
139
118
122
136
190
192
194
120
196
141
134
127
130
125
126
128
123
124
131
106
133

FIG. ~~6~~ 4

GENERAL RANGING PROCESS

FIG. ~~7A~~ 5A




FROM FIG. ~~7A~~ 5A
~~194~~
CU MONITORS GAP DURING PLURALITY OF SIGNATURE SEQUENCE FRAMES IN THE AUTHENTICATION INTERVAL AND PERFORMS CORRELATIONS DURING EACH GAP.
~~196~~ 197
CU COUNTS THE NUMBER OF GAPS IN AUTHENTICATION INTERVAL THAT HAVE ACTIVITY AND COMPARES THAT NUMBER TO THE TOTAL NUMBER OF FRAMES IN THE AUTHENTICATION INTERVAL TO DETERMINE IF THE 50% ACTIVITY LEVEL LIMIT HAS BEEN EXCEEDED.
GREATER THAN 50% ACTIVITY
204
CU BROADCASTS MESSAGE TO ALL RU'S INSTRUCTING ALL RU'S ATTEMPTING SYNCHRONIZATION TO EXECUTE THEIR COLLISION RESOLUTION PROTOCOLS.
50% ACTIVITY DETECTED
199 ~~198~~
CU IDENTIFIES RU FROM SIGNATURE AND BROADCASTS IDENTITY SO DETERMINED.
206
EACH RU ATTEMPTING TO SYNCHRONIZE EXECUTES A RANDOM DECISION WHETHER TO CONTINUE ATTEMPTING TO SYNCHRONIZE OR TO STOP, WITH A 50% PROBABILITY OF EITHER OUTCOME.
200
RU WITH IDENTITY BROADCAST BY CU RECOGNIZES ITS IDENTITY IN BROADCAST AND ENTERS FINE TUNING MODE.
202
CU INSTRUCTS RU ON HOW TO ADJUST ITS DELAY IN ORDER TO CENTER THE CORRELATION PEAK IN THE MIDDLE OF THE GAP/GUARDBAND.
208
RU'S THAT HAVE DECIDED TO CONTINUE RETRANSMIT THEIR SIGNATURE WITH THE SAME TIMING AS WAS USED ON THE LAST ITERATION
TO FIG. ~~7C~~ 5C

5B
FIG. ~~7B~~

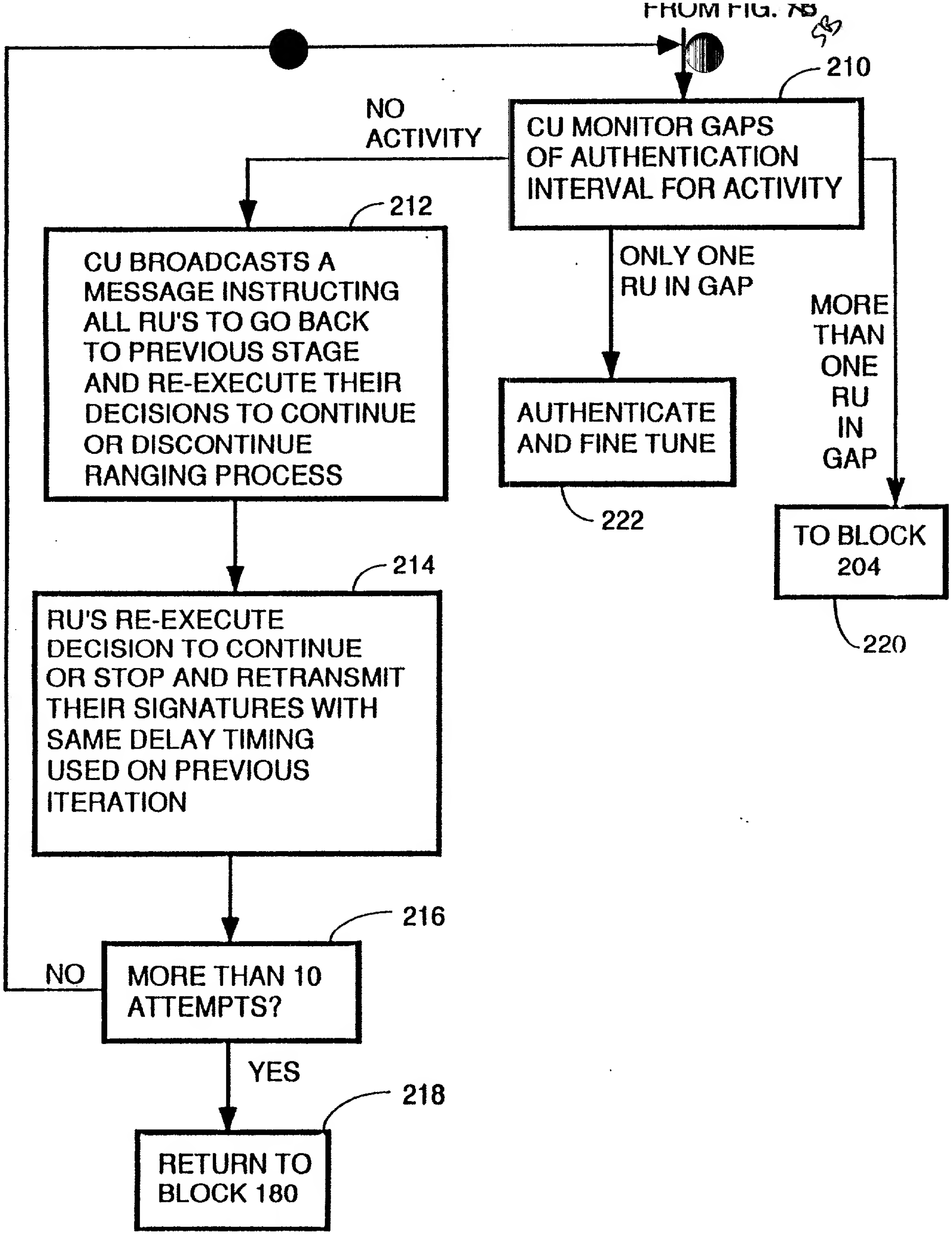

FROM FIG. ~~7B~~ 5B
210
CU MONITOR GAPS OF AUTHENTICATION INTERVAL FOR ACTIVITY
NO ACTIVITY
212
CU BROADCASTS A MESSAGE INSTRUCTING ALL RU'S TO GO BACK TO PREVIOUS STAGE AND RE-EXECUTE THEIR DECISIONS TO CONTINUE OR DISCONTINUE RANGING PROCESS
ONLY ONE RU IN GAP
AUTHENTICATE AND FINE TUNE
222
MORE THAN ONE RU IN GAP
TO BLOCK 204
220
214
RU'S RE-EXECUTE DECISION TO CONTINUE OR STOP AND RETRANSMIT THEIR SIGNATURES WITH SAME DELAY TIMING USED ON PREVIOUS ITERATION
216
NO
MORE THAN 10 ATTEMPTS?
YES
218
RETURN TO BLOCK 180

FIG. ~~7C~~ 5C

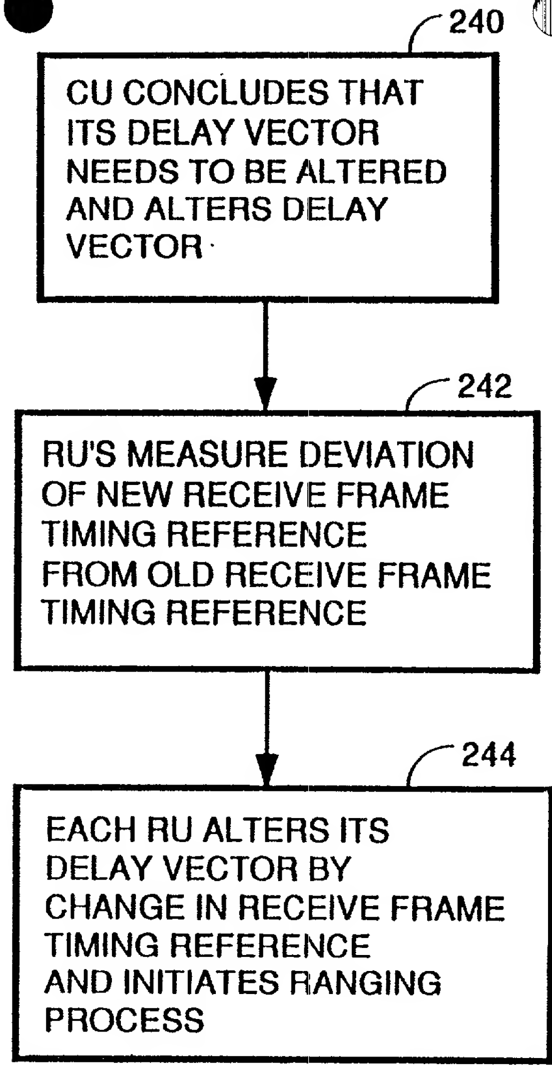


FIG. ~~8~~ 6
DEAD RECKONING RE-SYNC

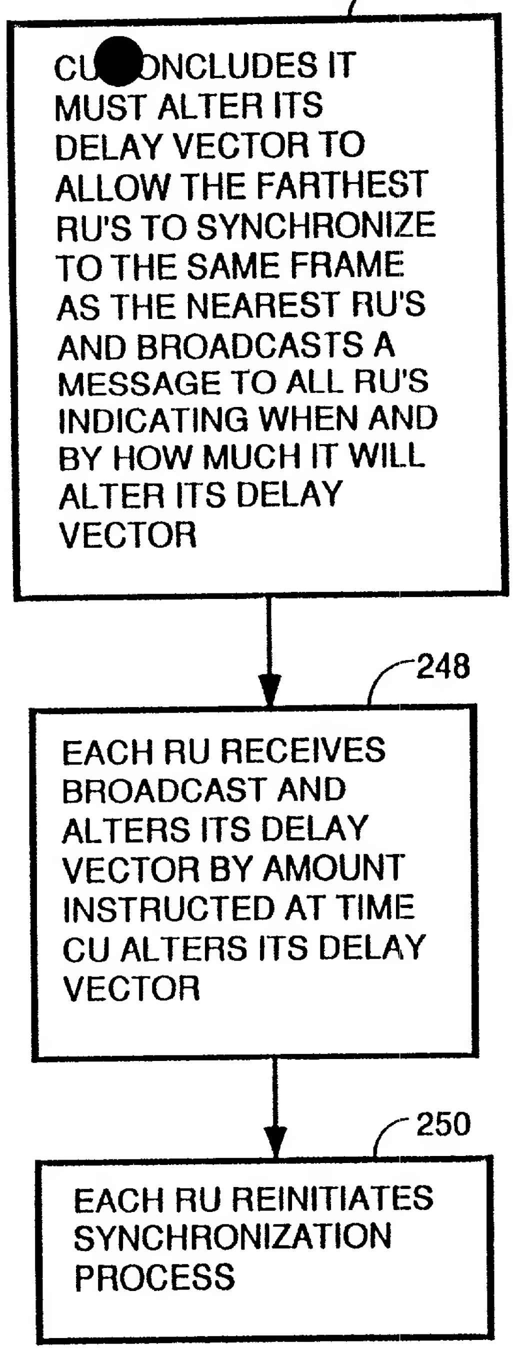
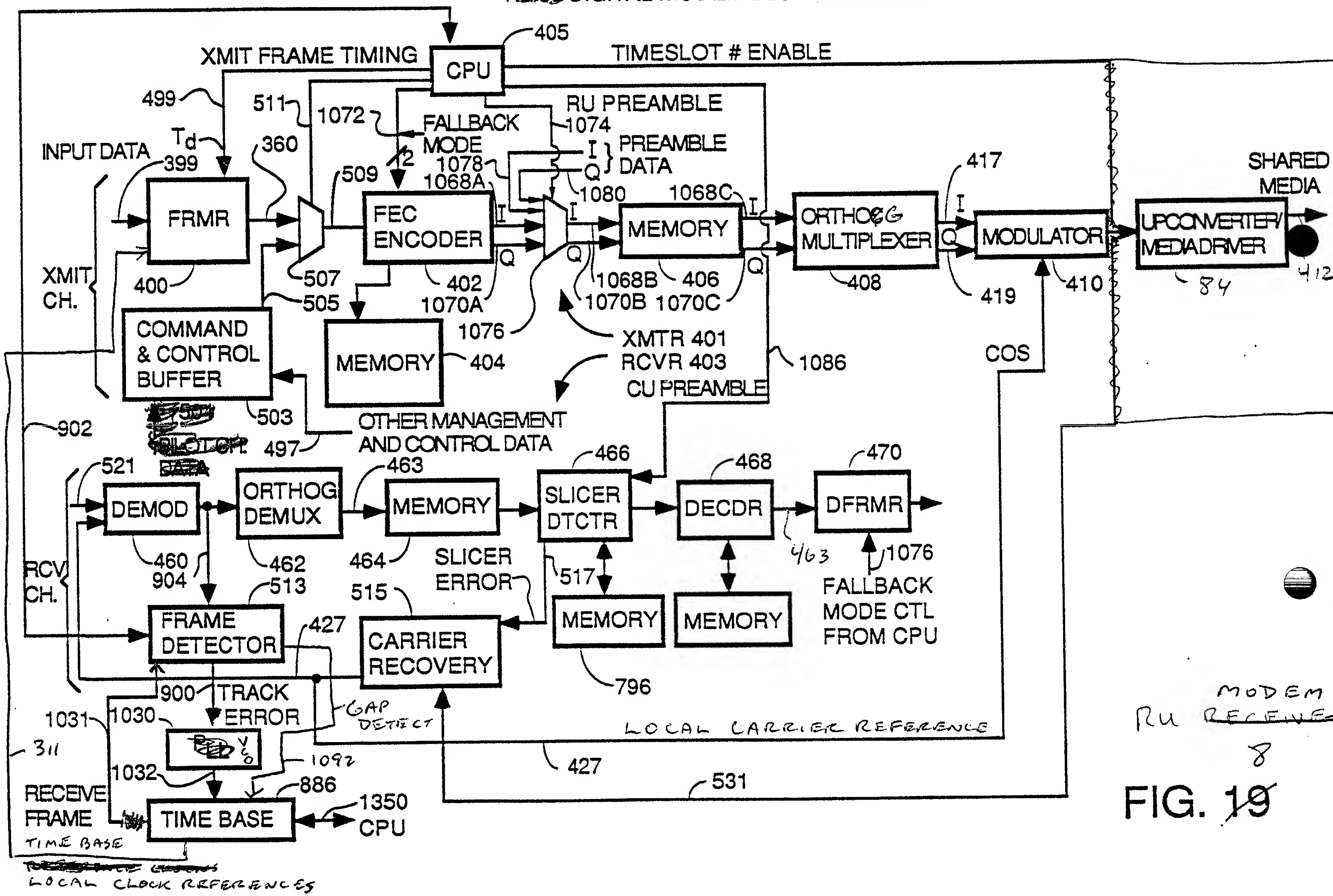


FIG. ~~9~~ 7

PRECURSOR EMBODIMENT

RU ~~RDCU~~ DIGITAL MODEM BLOCK DIAGRAM



MODEM RU ~~RECEIVER~~

FIG. ~~19~~ 8

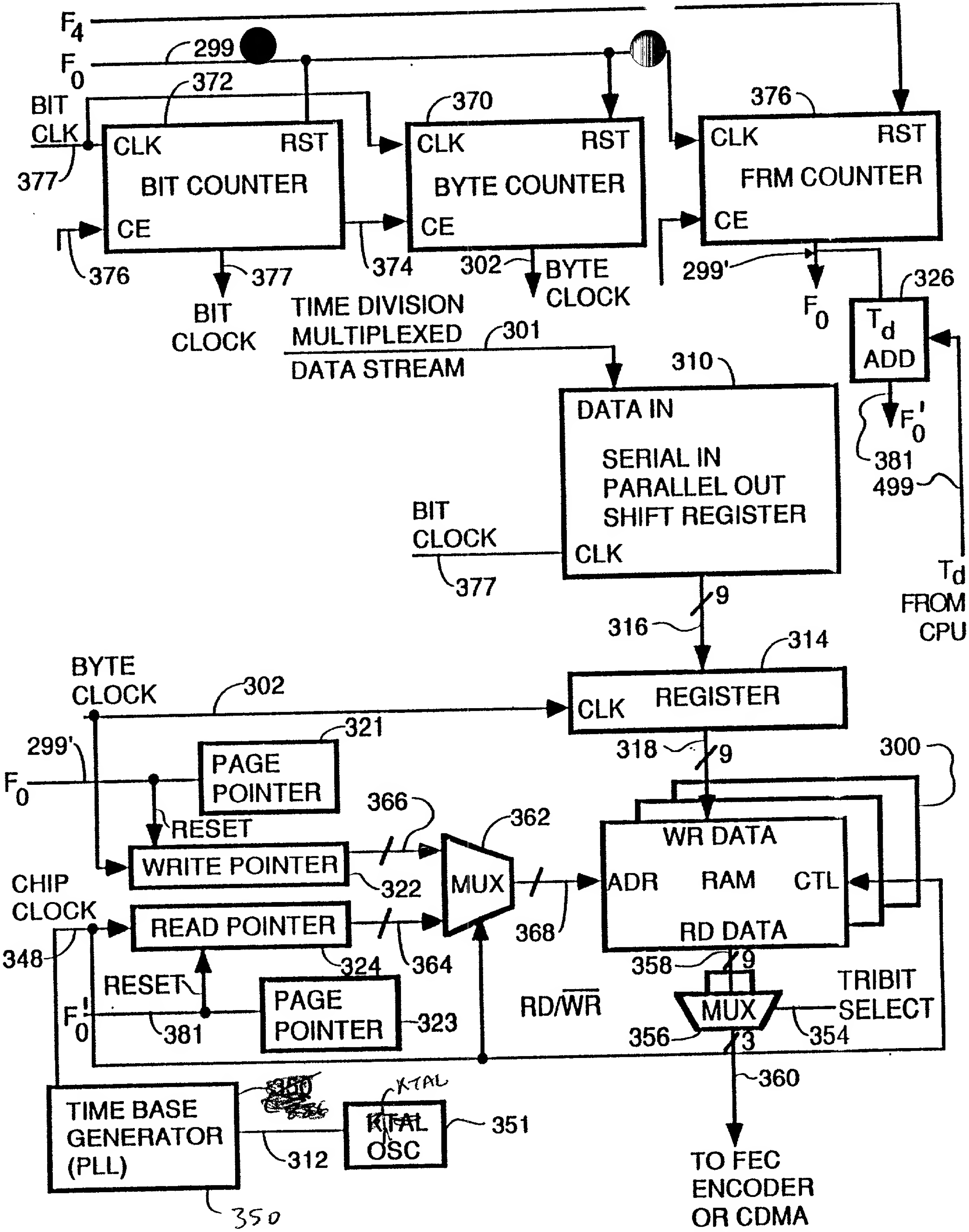

F4
F0
299
BIT CLK
372
377
CLK
RST
BIT COUNTER
CE
376
377
BIT CLOCK
370
BYTE COUNTER
374
302
BYTE CLOCK
376
FRM COUNTER
299'
F0
326
Td ADD
TIME DIVISION MULTIPLEXED DATA STREAM
301
310
DATA IN
SERIAL IN PARALLEL OUT SHIFT REGISTER
F0'
381
499
BIT CLOCK
377
9
316
Td FROM CPU
314
BYTE CLOCK
302
REGISTER
321
299'
F0
PAGE POINTER
318
300
366
362
RESET
WRITE POINTER
MUX
WR DATA
ADR
RAM
CTL
322
CHIP CLOCK
READ POINTER
368
RD DATA
348
324
364
358
RESET
PAGE POINTER
323
RD/WR
TRIBIT SELECT
F0'
381
356
354
3
360
TIME BASE GENERATOR (PLL)
~~350~~
XTAL
~~XTAL~~ OSC
351
312
350
TO FEC ENCODER OR CDMA MUX/BUFFER

FIG. ~~12~~ 9

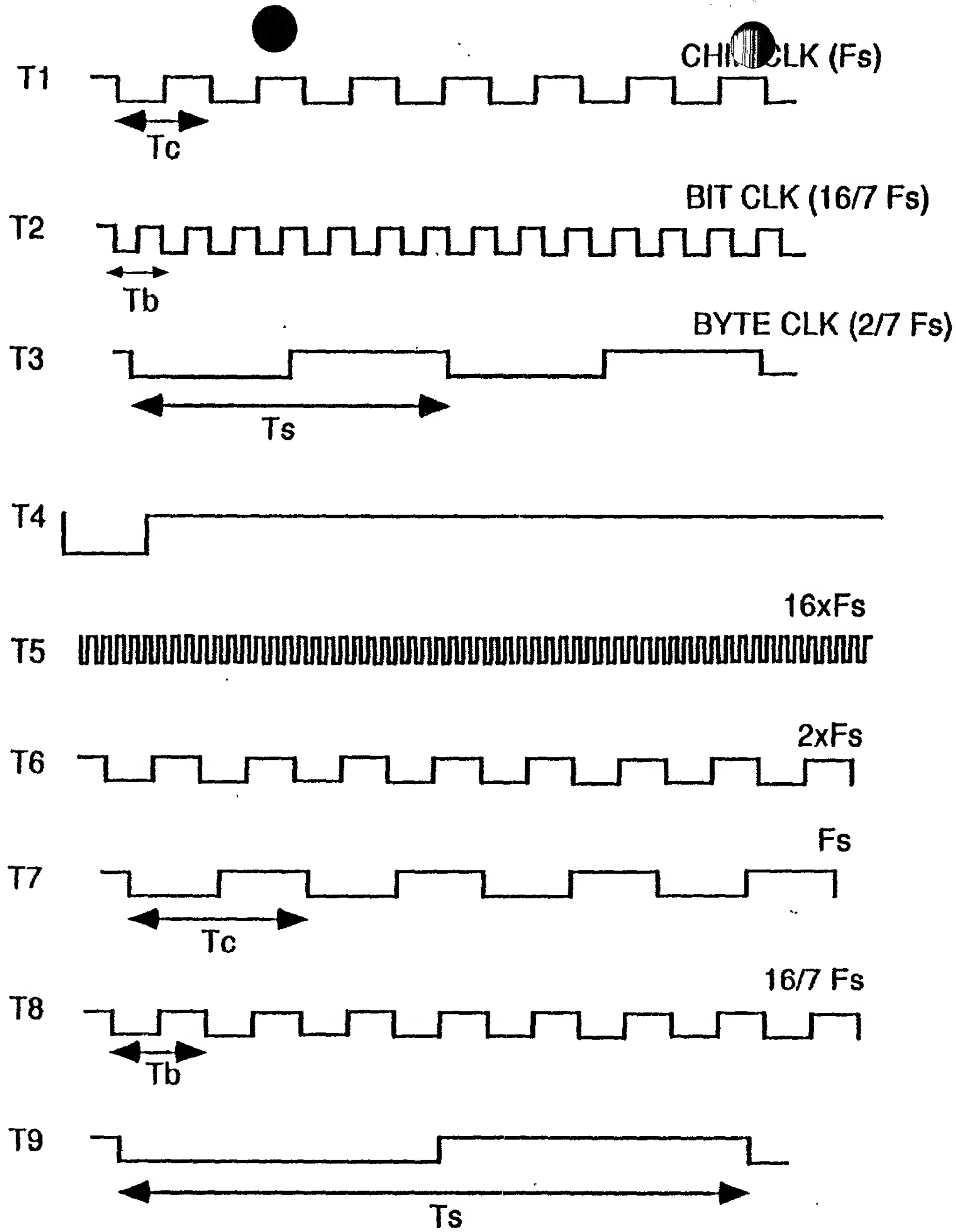

T1
CLK (Fs)
Tc
T2
BIT CLK (16/7 Fs)
Tb
T3
BYTE CLK (2/7 Fs)
Ts
T4
T5
16xFs
T6
2xFs
T7
Fs
Tc
T8
16/7 Fs
Tb
T9
Ts

FIG. ~~13~~ 10

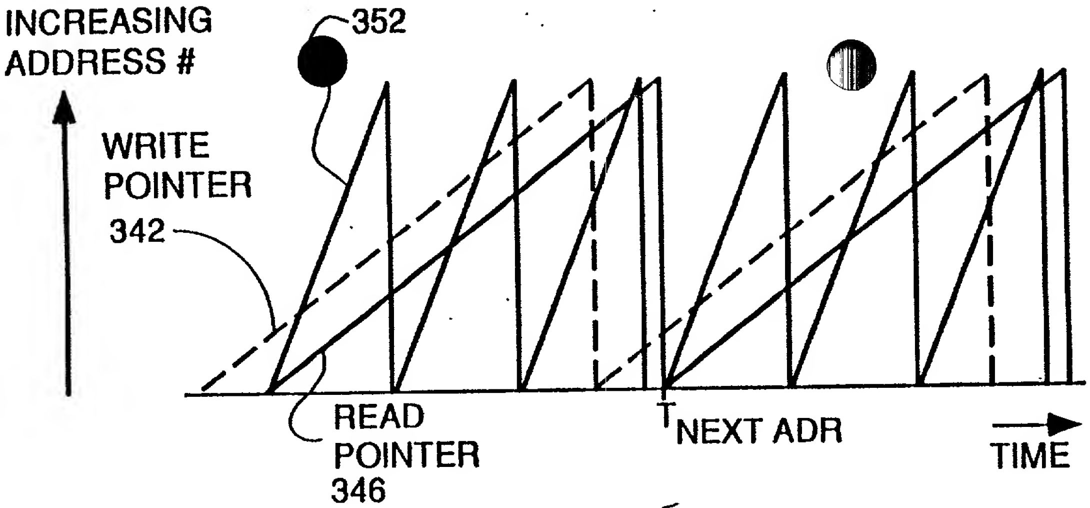


FIG. ~~17~~ 15

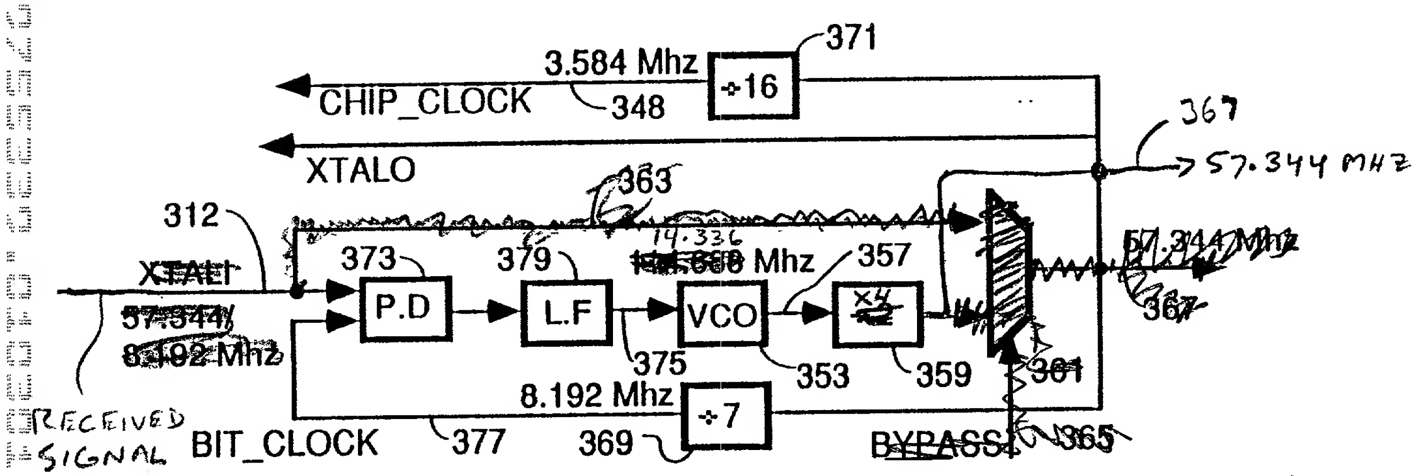


FIG. ~~18~~ 11

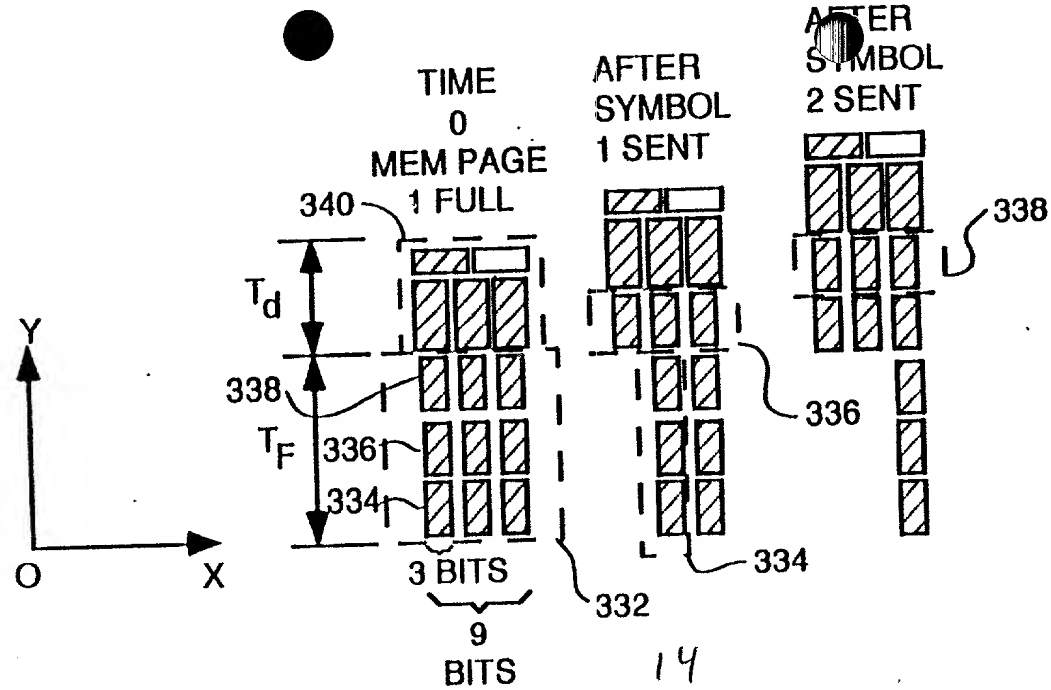


FIG. ~~14~~ 14 ok

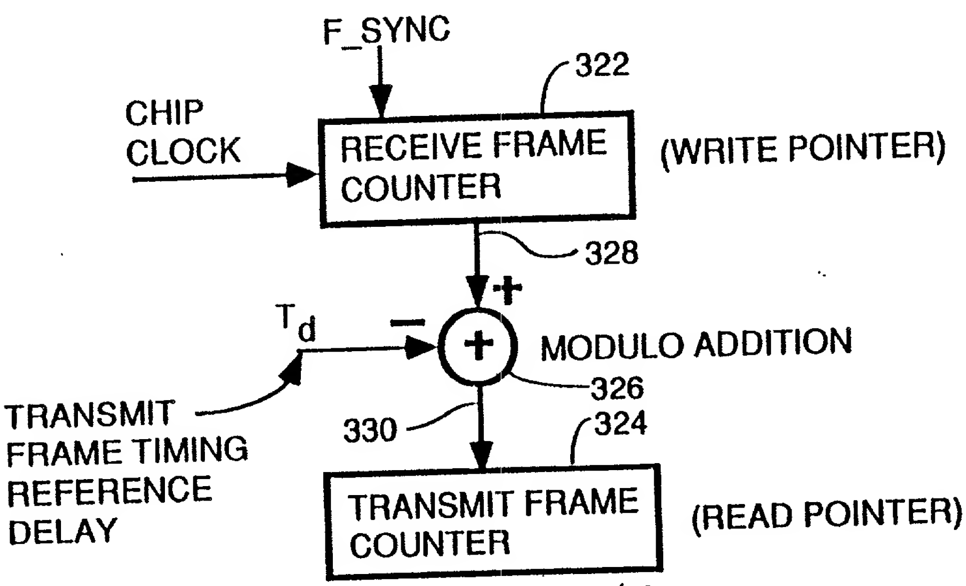


FIG. ~~15~~ 12

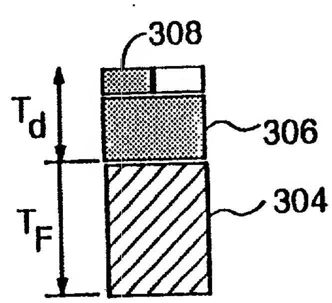


FIG. ~~16~~ 13

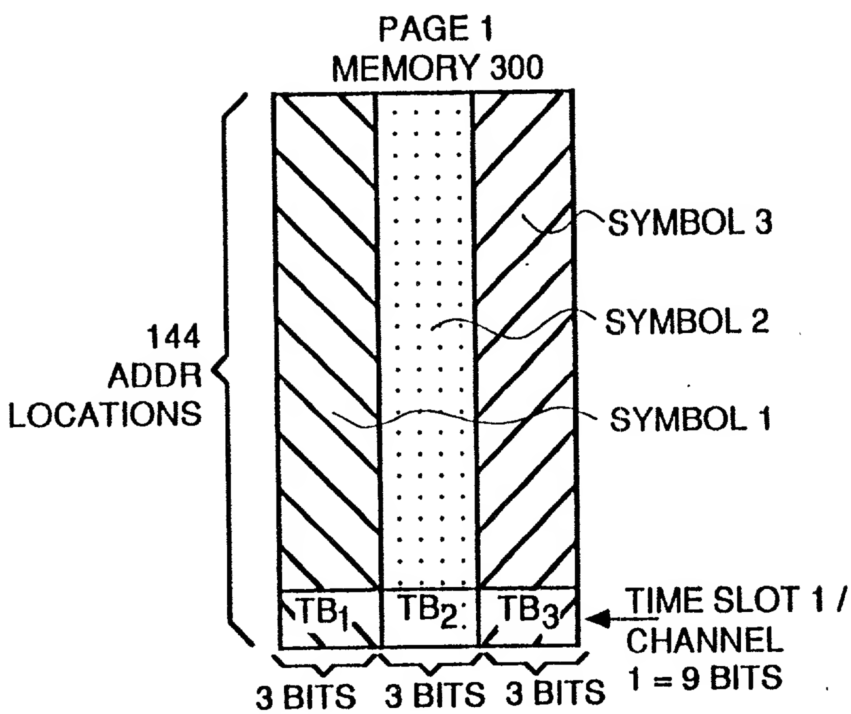
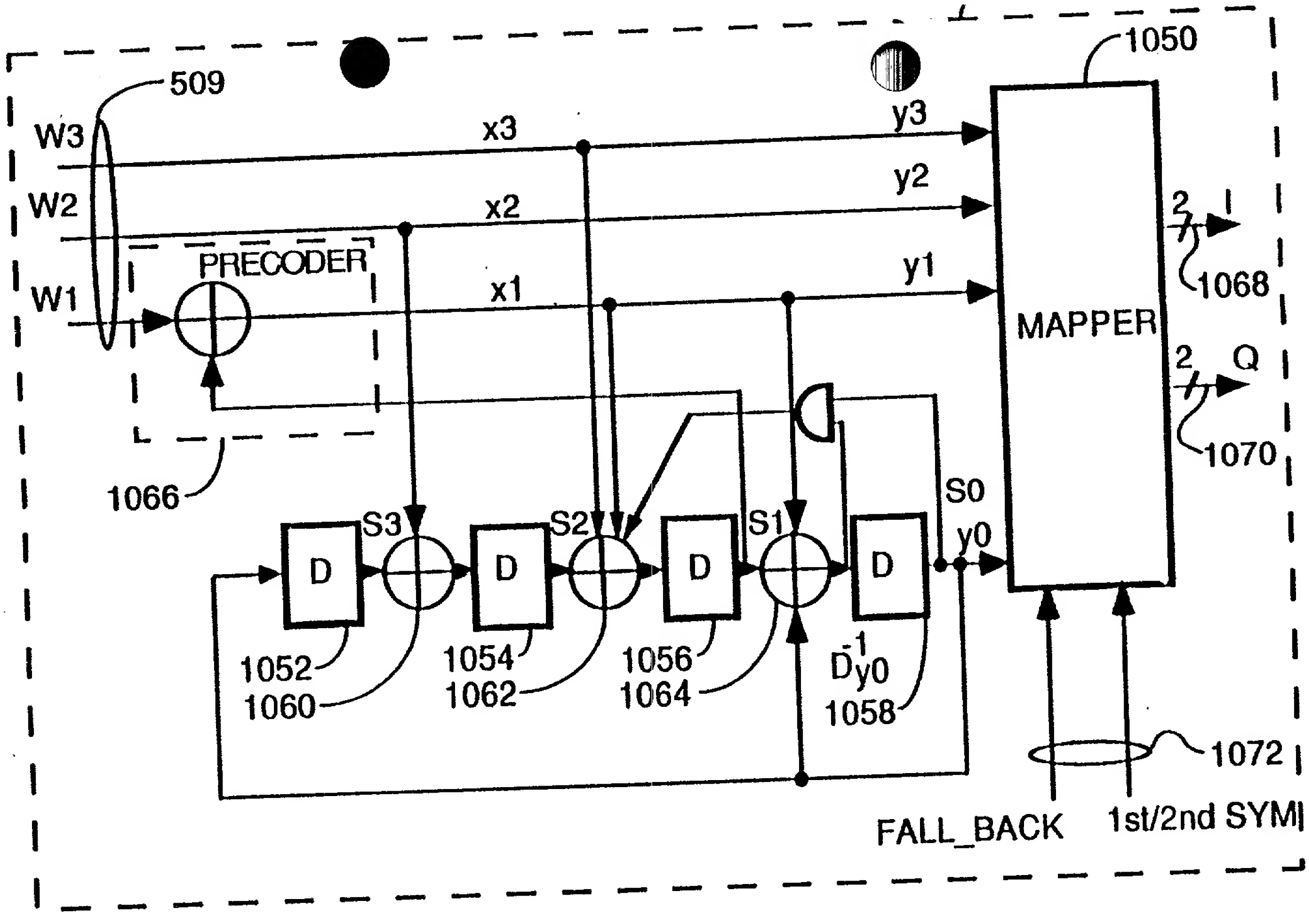

PAGE 1
MEMORY 300
144
ADDR
LOCATIONS
SYMBOL 3
SYMBOL 2
SYMBOL 1
TB_1
TB_2
TB_3
TIME SLOT 1 /
CHANNEL
1 = 9 BITS
3 BITS
3 BITS
3 BITS

FIG. ~~20~~ 16



PREFERRED TRELLIS ENCODER

FIG. ~~42~~ 17

MAPPING FOR FALL-BACK MODE - LSB'S

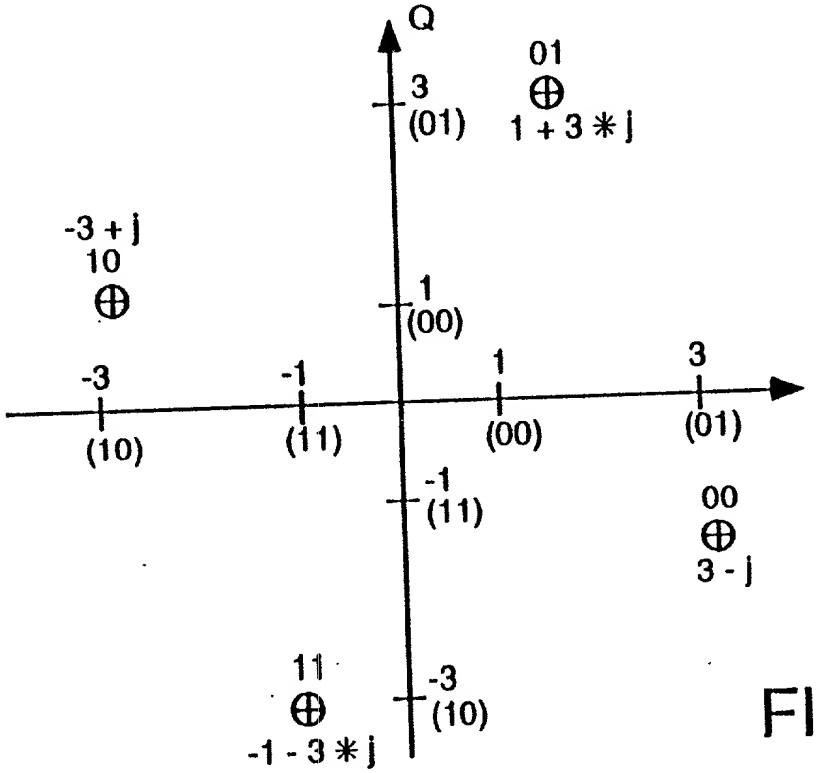


FIG. ~~43~~ 21

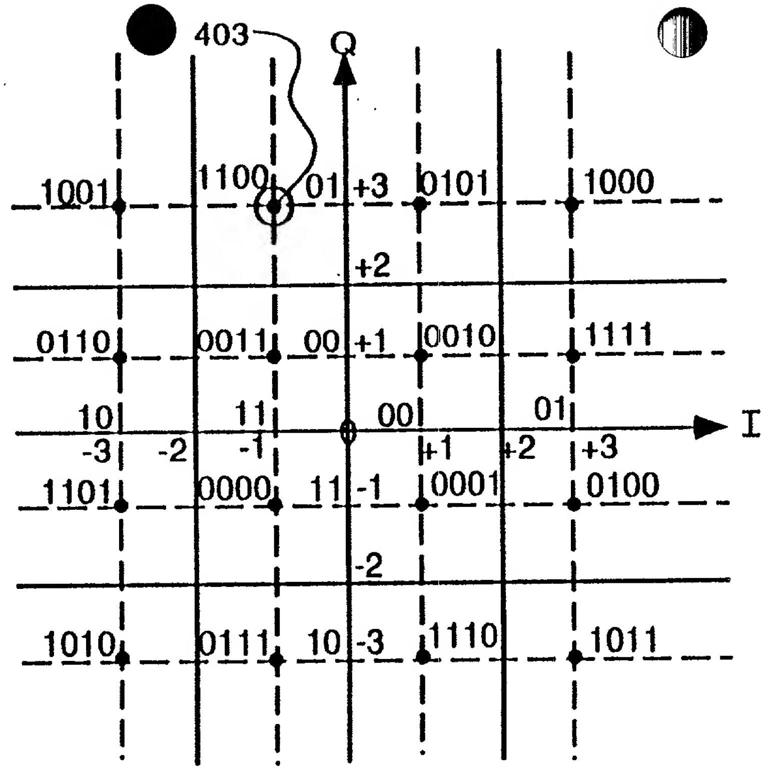
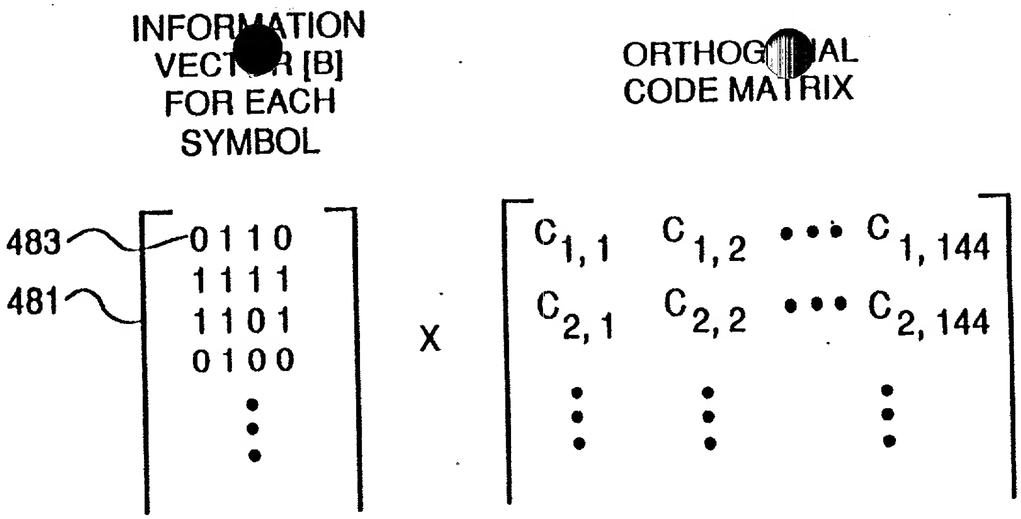


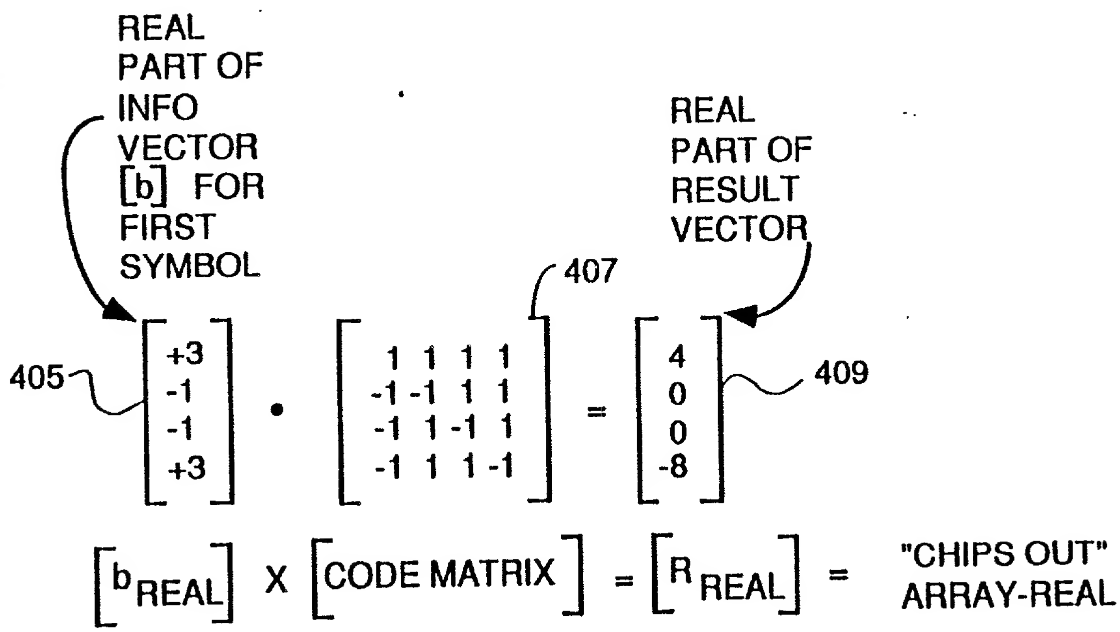
FIG. ~~21~~ 18

	CODE	INPHASE	QUADRATURE	
	0000	111	111	= -1 -
	0001	001	111	= 1 - j
	0010	001	001	= 1+ j
	0011	111	001	= -1+ j
	0100	011	111	= 3 - j
	0101	001	011	= 1+ 3*j
	0110	101	001	= -3 + j
	0111	111	101	= -1 - 3* j
	1000	011	011	=+3 + 3*j
	1001	101	011	= -3 + 3*j
	1010	101	101	= -3 - 3* j
	1011	011	101	= 3 - 3* j
403	1100	111	011	= -1+ 3* j
	1101	101	111	= -3 - j
	1110	001	101	= 1 - 3* j
	1111	011	001	= 3 + j

FIG. ~~22~~ 19



20 A
FIG. ~~23~~A



20 B
FIG. ~~23~~B

LSBs y1 y0	PHASE	1+jQ
00	0	3-j
01	90	1+j3
10	180	-3+j
11	-90	-1-j3

MSBs y3 y2	PHASE difference (2nd-1st symbol)	1+jQ WHEN LSB=00	1+jQ WHEN LSB=01	1+jQ WHEN LSB=10	1+jQ WHEN LSB=11
00	0	3-j	1+j3	-3+j	-1-j3
01	90	1+j3	-3+j	-1-j3	3-j
10	180	-3+j	-1-j3	3-j	1+j3
11	-90	-1-j3	3-j	1+j3	-3+j

LSB & MSB FALLBACK MODE MAPPINGS

FIG. ~~44~~ 22

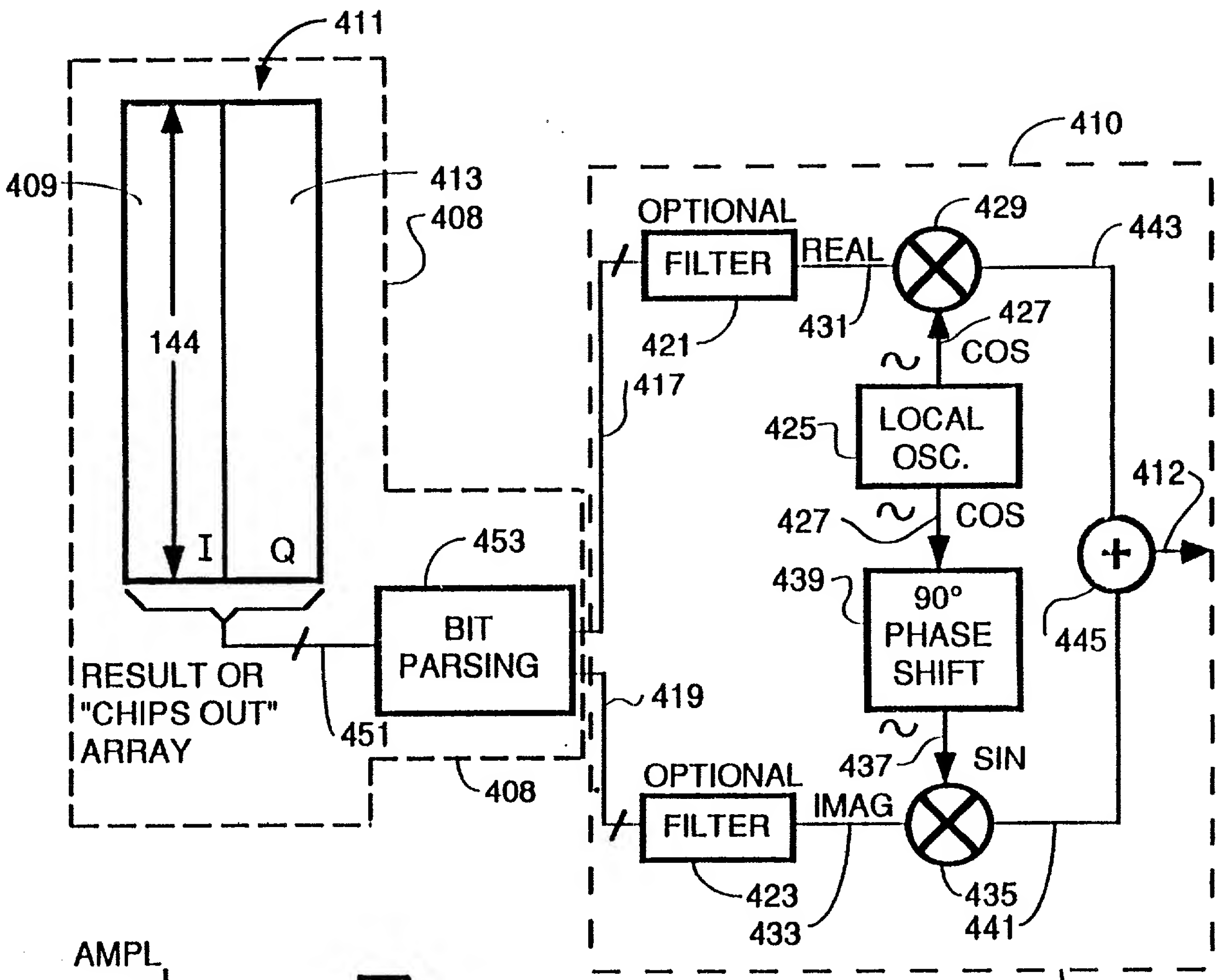


FIG. ~~24~~ 23

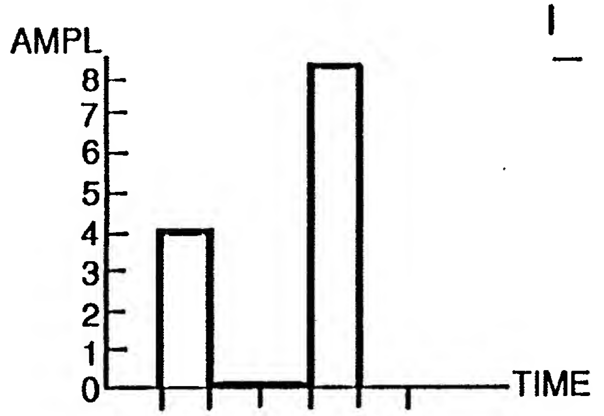
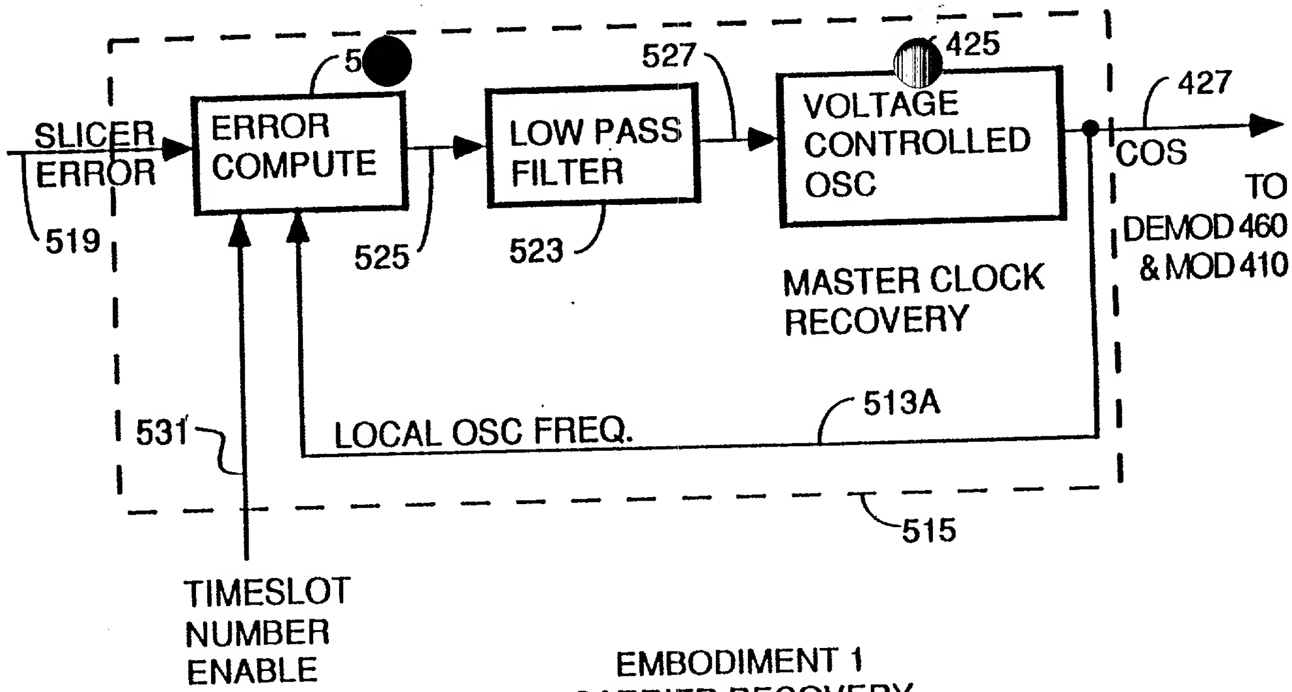
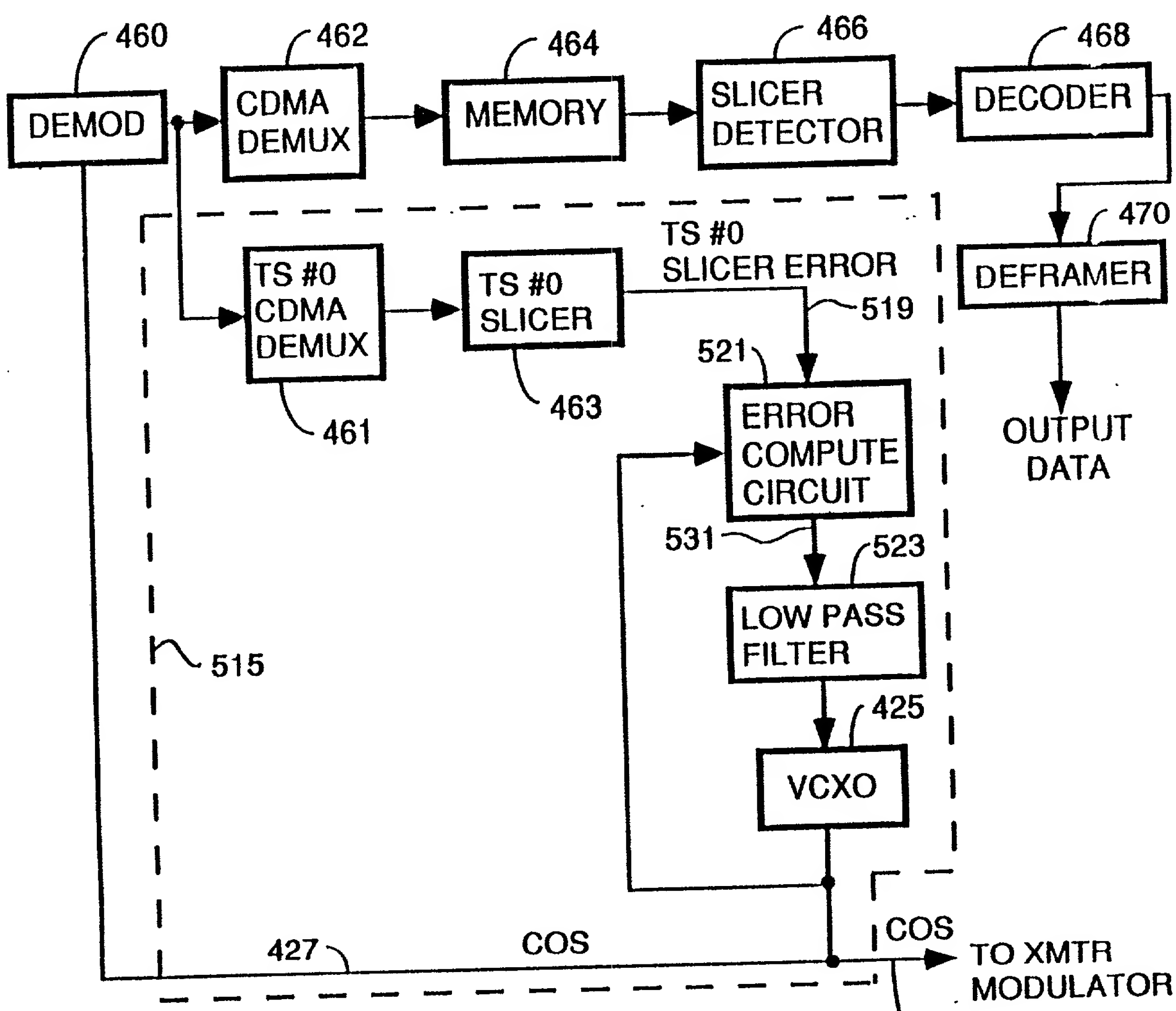


FIG. ~~25~~ 24



EMBODIMENT 1
CARRIER RECOVERY

FIG. ~~35~~ 25



EMBODIMENT 2 CARRIER RECOVERY

FIG. ~~36~~ 26

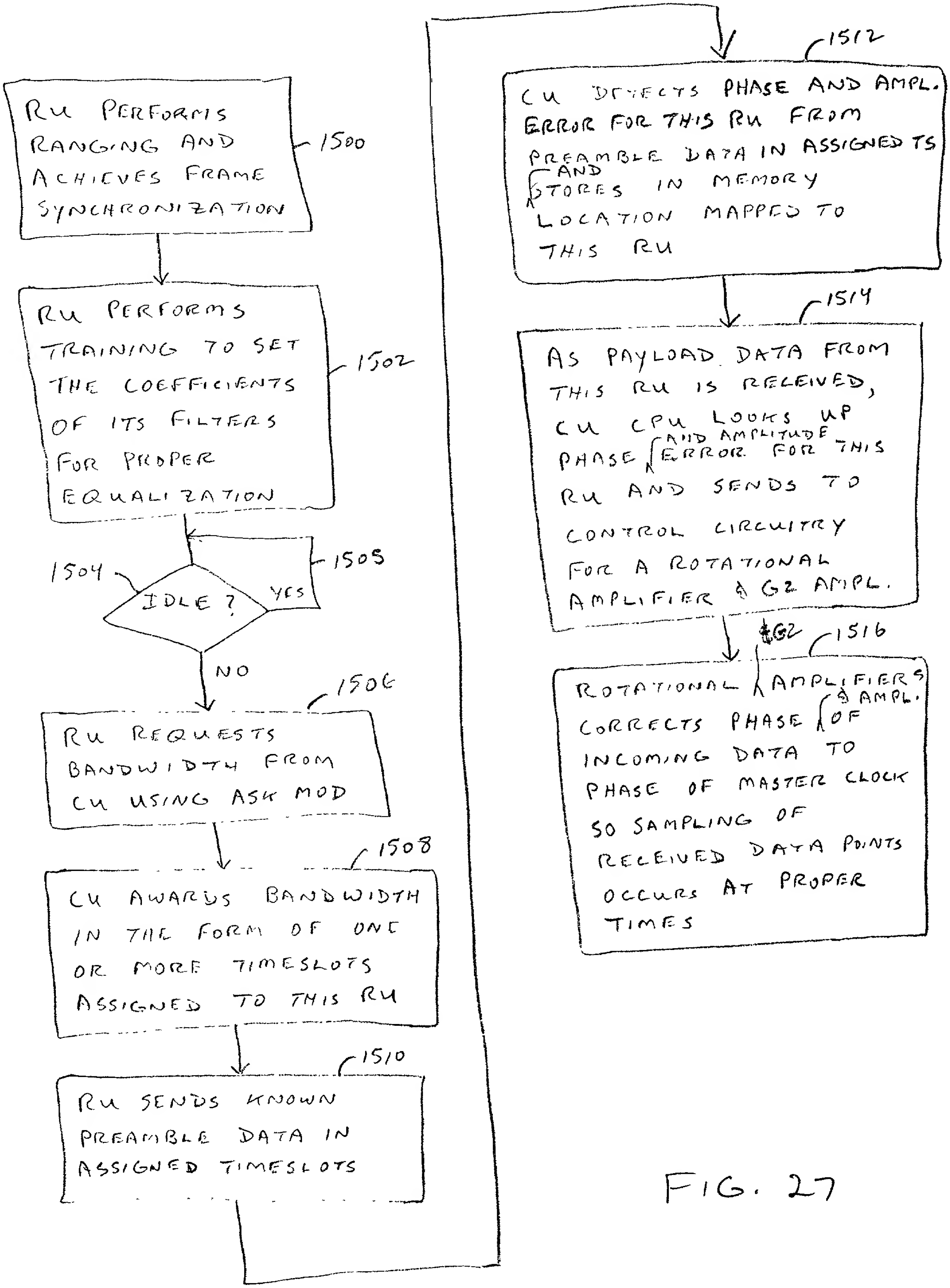
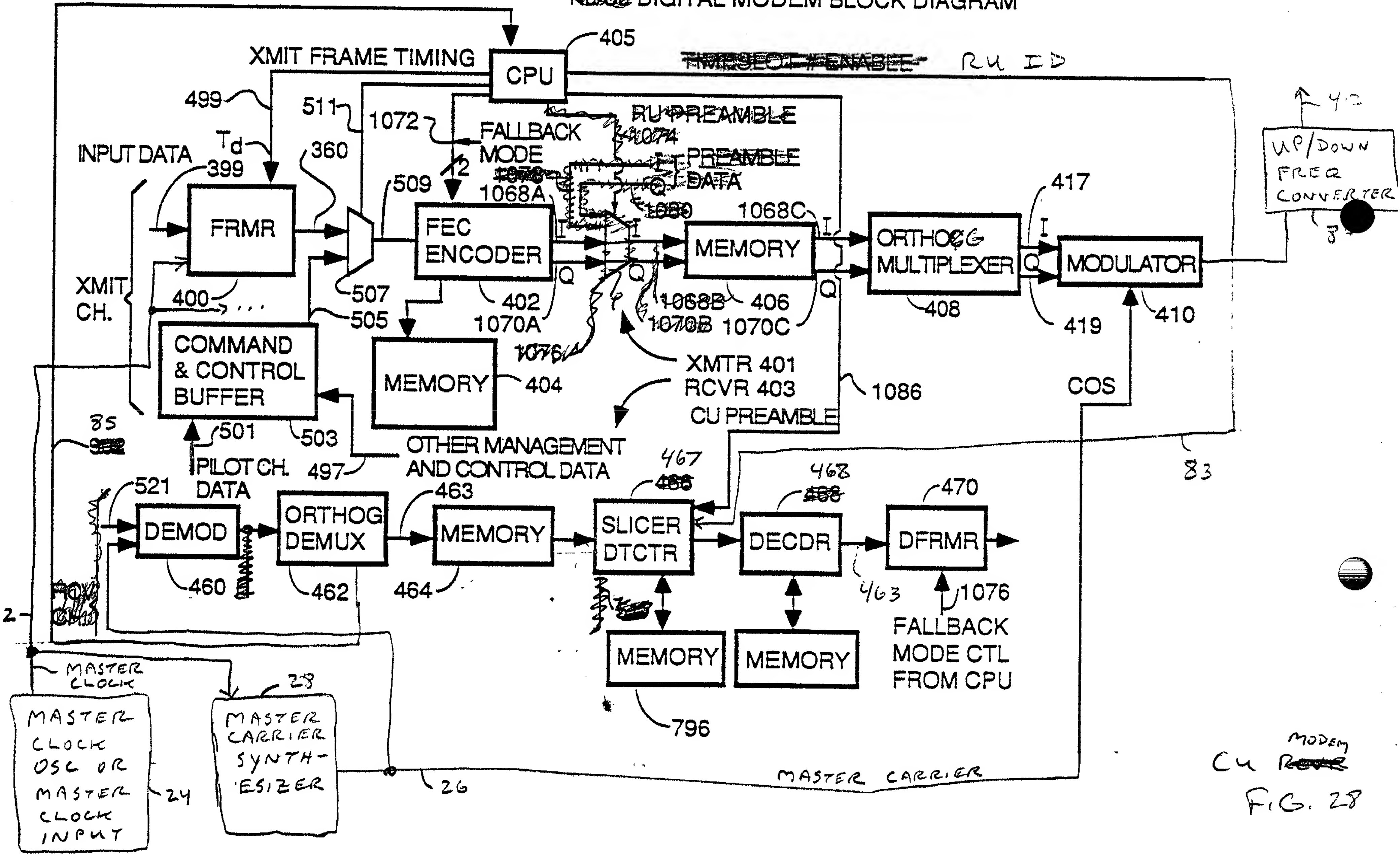

RU PERFORMS RANGING AND ACHIEVES FRAME SYNCHRONIZATION
1500
RU PERFORMS TRAINING TO SET THE COEFFICIENTS OF ITS FILTERS FOR PROPER EQUALIZATION
1502
1504
IDLE ?
YES
1505
NO
RU REQUESTS BANDWIDTH FROM CU USING ASK MOD
1506
CU AWARDS BANDWIDTH IN THE FORM OF ONE OR MORE TIMESLOTS ASSIGNED TO THIS RU
1508
RU SENDS KNOWN PREAMBLE DATA IN ASSIGNED TIMESLOTS
1510
CU DETECTS PHASE AND AMPL. ERROR FOR THIS RU FROM PREAMBLE DATA IN ASSIGNED TS AND STORES IN MEMORY LOCATION MAPPED TO THIS RU
1512
AS PAYLOAD DATA FROM THIS RU IS RECEIVED, CU CPU LOOKS UP PHASE AND AMPLITUDE ERROR FOR THIS RU AND SENDS TO CONTROL CIRCUITRY FOR A ROTATIONAL AMPLIFIER & G2 AMPL.
1514
& G2
ROTATIONAL AMPLIFIERS CORRECTS PHASE & AMPL. OF INCOMING DATA TO PHASE OF MASTER CLOCK SO SAMPLING OF RECEIVED DATA POINTS OCCURS AT PROPER TIMES
1516

FIG. 27

DIGITAL MODEM BLOCK DIAGRAM



CU MODEM
FIG. 28

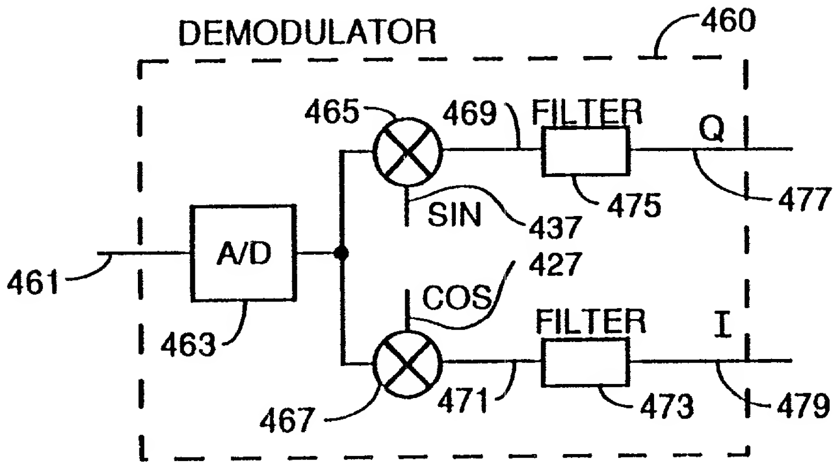
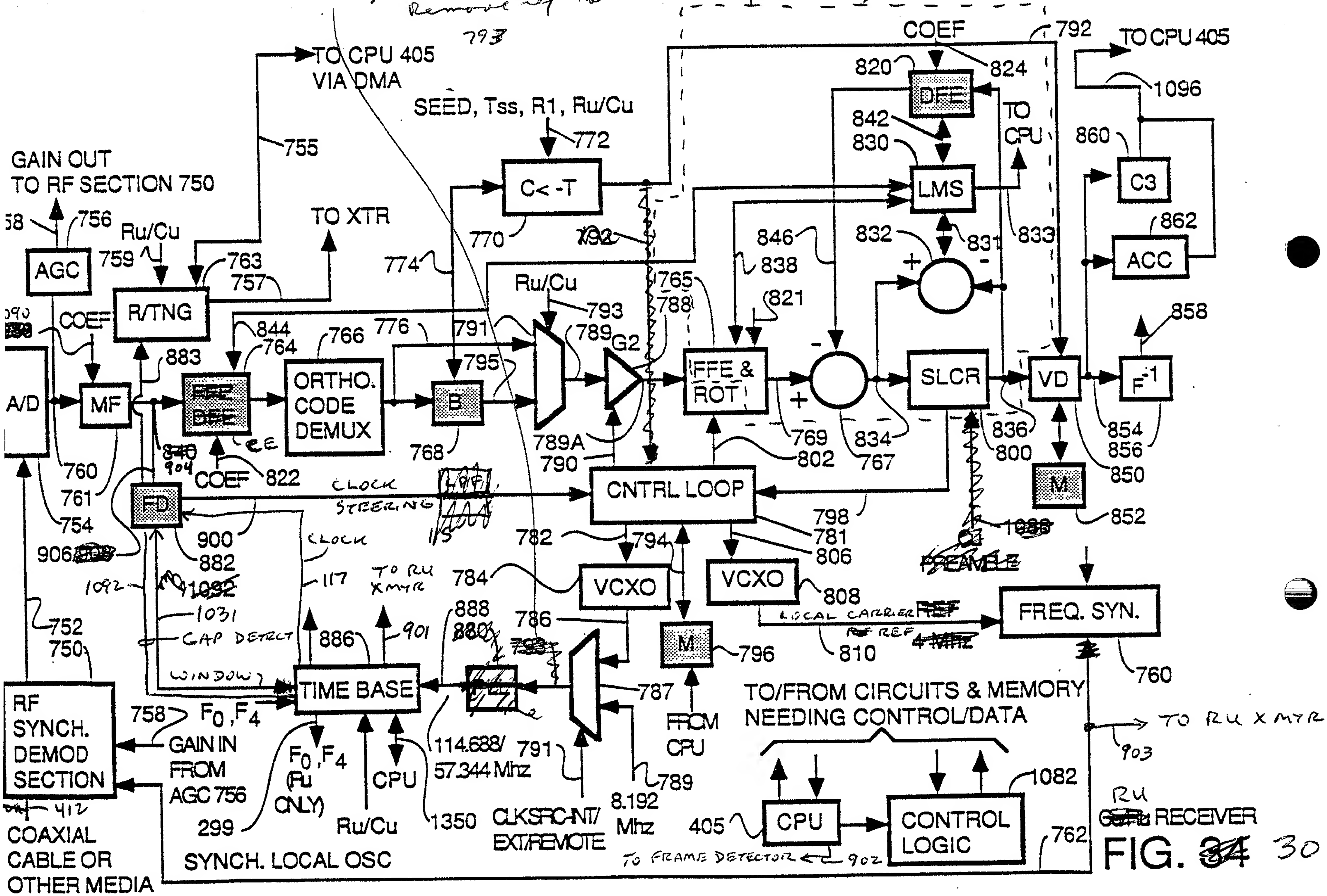

DEMODULATOR
460
465
469
FILTER
Q
477
475
SIN
437
461
A/D
427
COS
FILTER
I
463
467
471
473
479

FIG. ~~26~~ 29

Page 94, Line 8 Remove ref to 793



RU RECEIVER

FIG. ~~34~~ 30

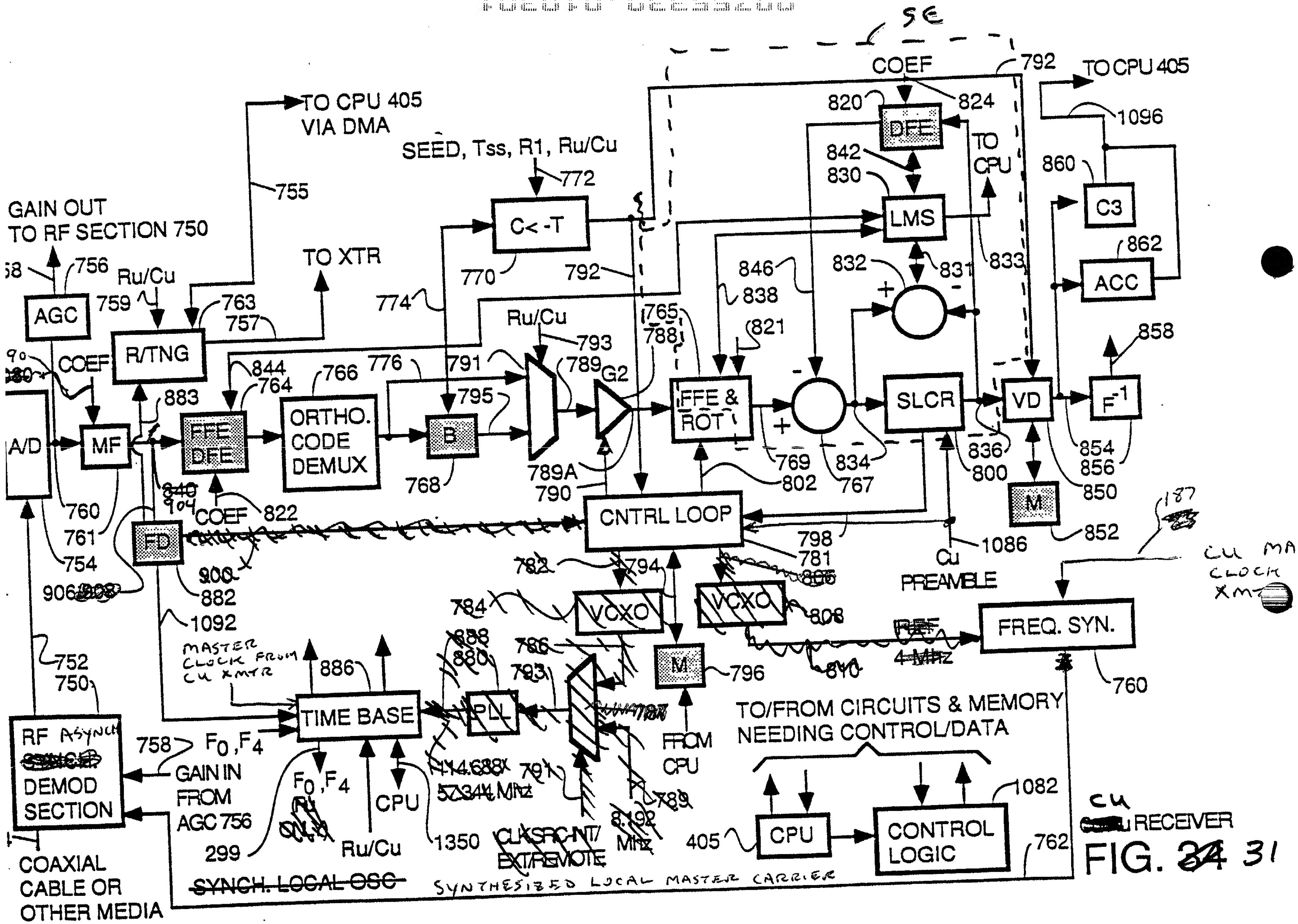
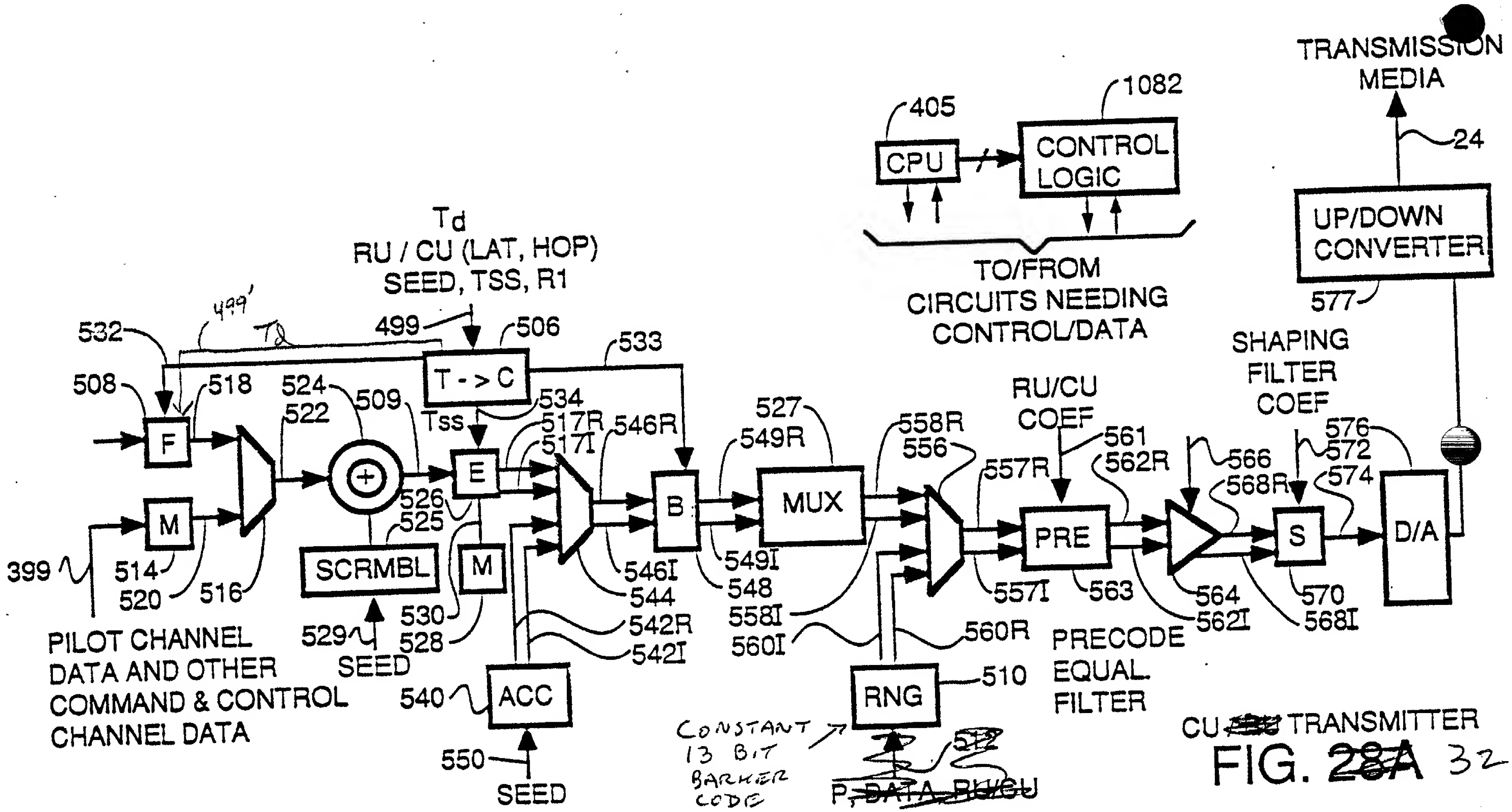

SE
GAIN OUT TO RF SECTION 750
AGC
MF
A/D
R/TNG
FFE DFE
FD
ORTHO. CODE DEMUX
B
C< -T
SEED, Tss, R1, Ru/Cu
TO CPU 405 VIA DMA
TO XTR
COEF
Ru/Cu
G2
FFE & ROT
CNTRL LOOP
VCXO
M
PLL
TIME BASE
DFE
LMS
SLCR
VD
C3
ACC
TO CPU 405
TO CPU
Cu PREAMBLE
FREQ. SYN.
4 Mhz
TO/FROM CIRCUITS & MEMORY NEEDING CONTROL/DATA
CPU
CONTROL LOGIC
FROM CPU
RF ASYNCH DEMOD SECTION
GAIN IN FROM AGC 756
COAXIAL CABLE OR OTHER MEDIA
~~SYNCH. LOCAL OSC~~
SYNTHESIZED LOCAL MASTER CARRIER
MASTER CLOCK FROM CU XMTR
CU MASTER CLOCK FROM XMTR
F_0, F_4
CLKSRC INT/EXT/REMOTE
8.192 MHz
57.344 MHz
CU RECEIVER

FIG. ~~24~~ 31



CU ~~232~~ TRANSMITTER

FIG. ~~28A~~ 32

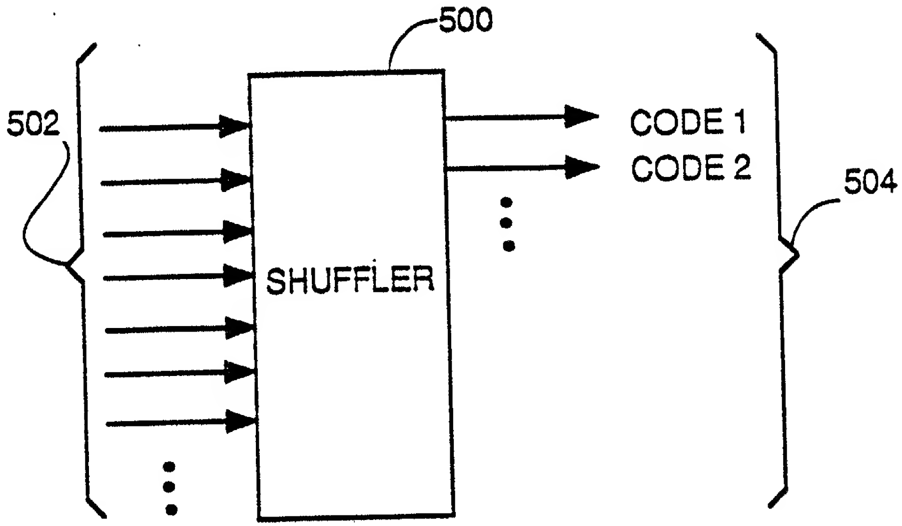
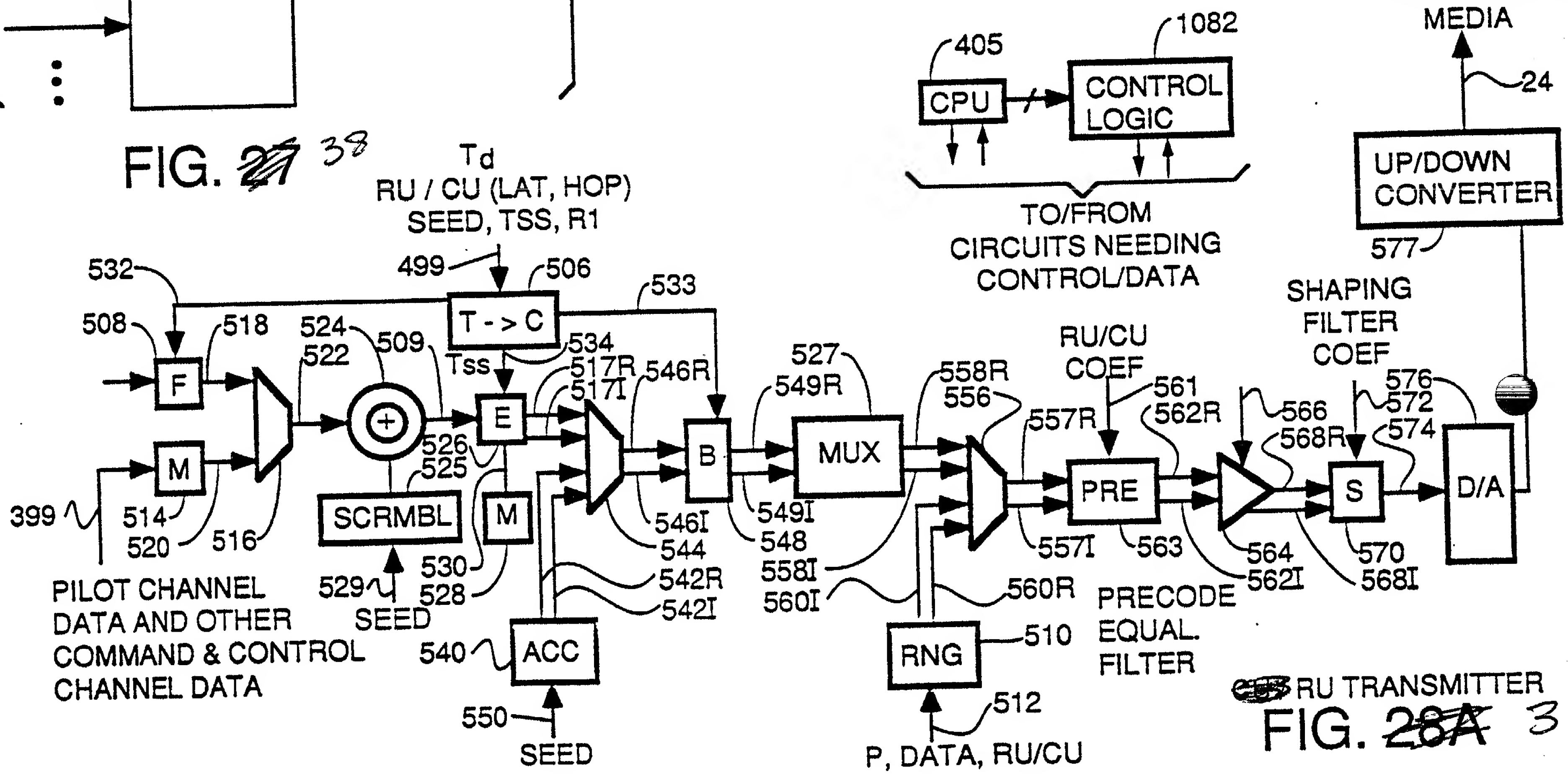
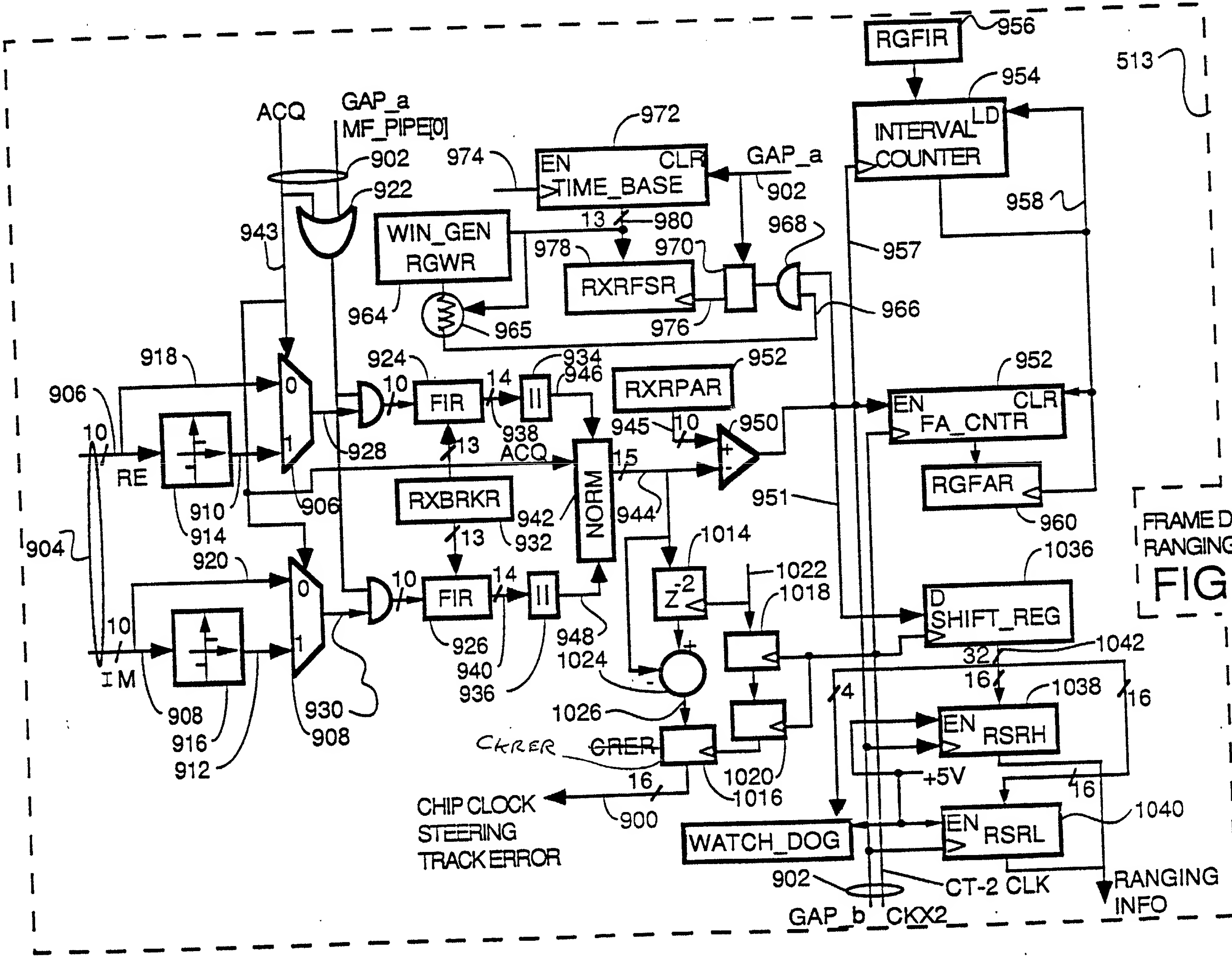


FIG. ~~27~~ 38



RU TRANSMITTER

FIG. ~~28A~~ 3



FRAME DETECTOR/ RANGING DETECTOR

FIG. ~~38~~

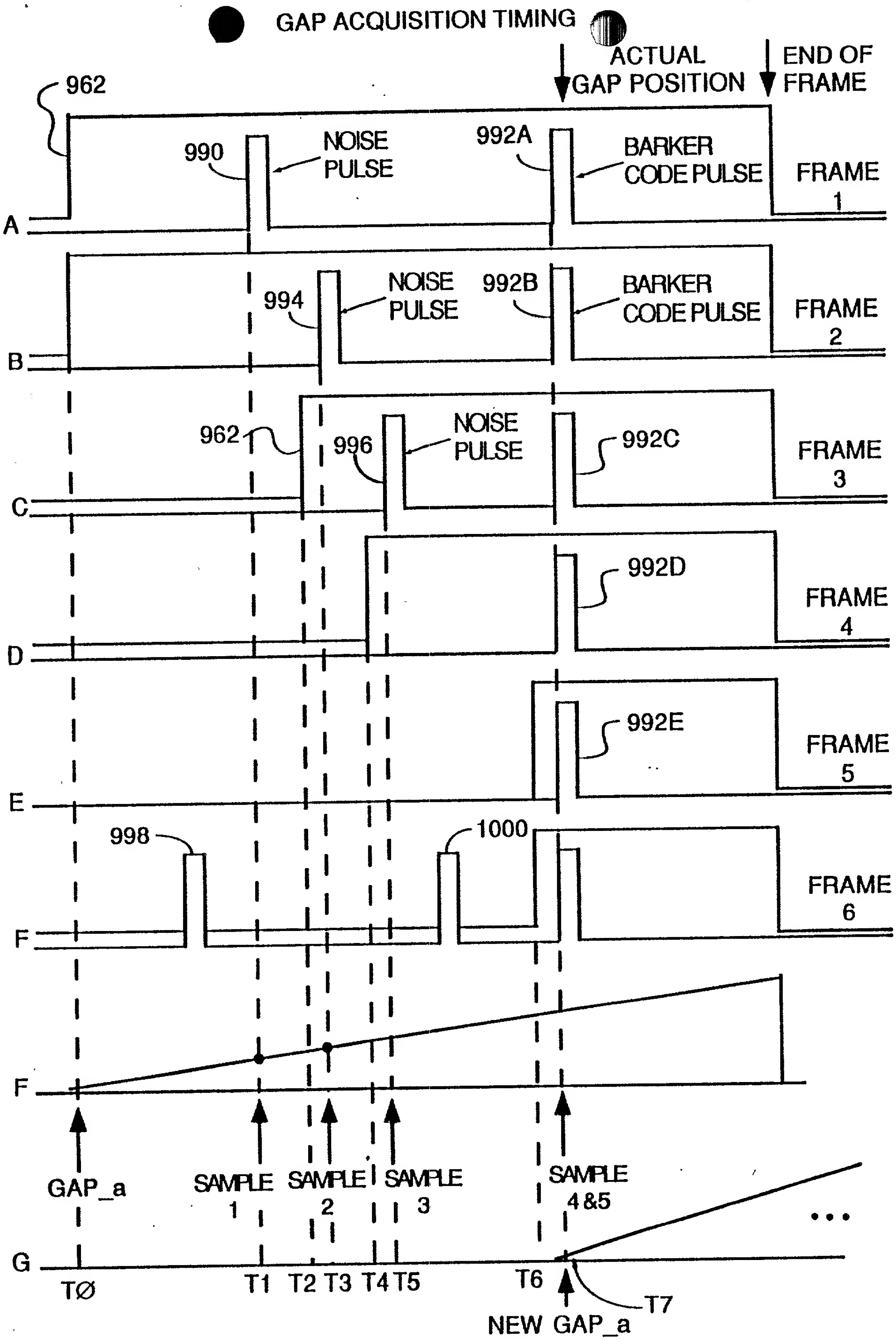
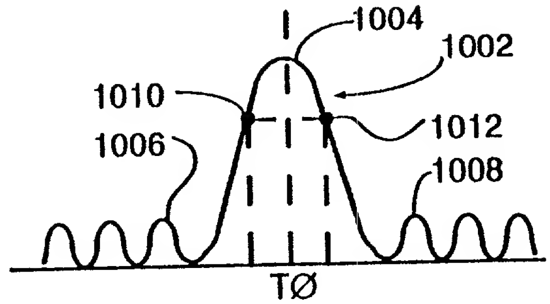
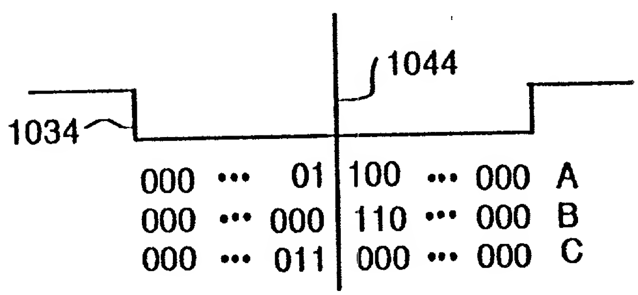

GAP ACQUISITION TIMING
ACTUAL GAP POSITION
END OF FRAME
962
990
NOISE PULSE
992A
BARKER CODE PULSE
FRAME 1
A
994
NOISE PULSE
992B
BARKER CODE PULSE
FRAME 2
B
962
996
NOISE PULSE
992C
FRAME 3
C
992D
FRAME 4
D
992E
FRAME 5
E
998
1000
FRAME 6
F
F
GAP_a
SAMPLE 1
SAMPLE 2
SAMPLE 3
SAMPLE 4 &5
G
TØ
T1
T2
T3
T4
T5
T6
T7
NEW GAP_a

FIG. ~~39~~ 35



36
FIG. ~~40~~



37
FIG. ~~41~~

FINE TUNING
TO CENTER
BARKER CODE

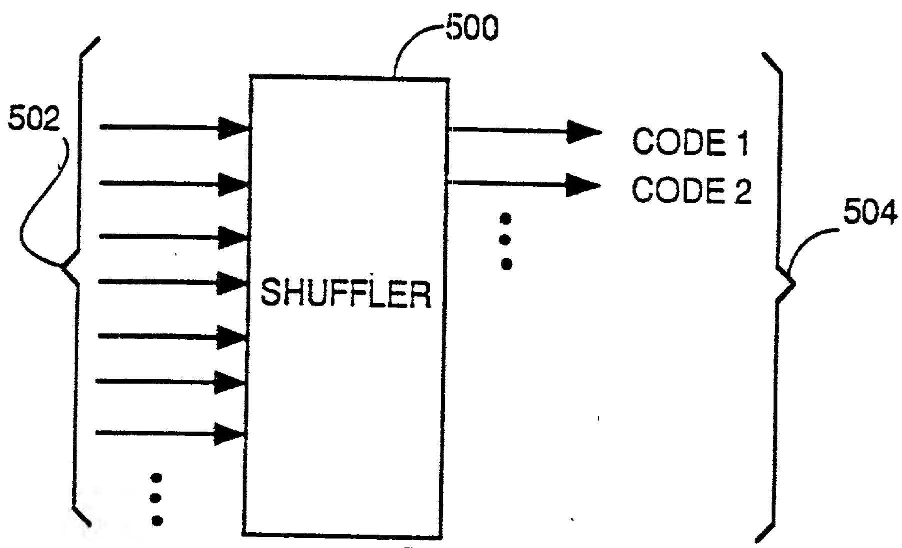


FIG. ~~27~~ 38

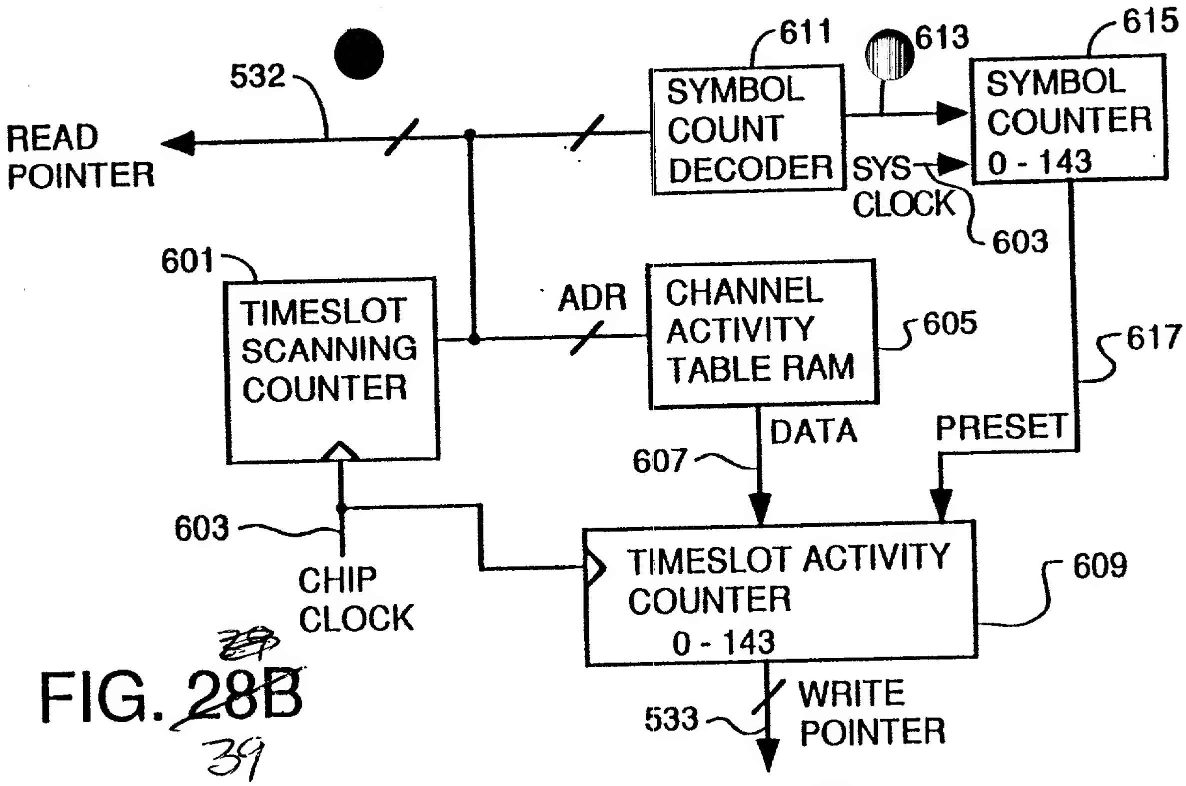


FIG. ~~28B~~ 39

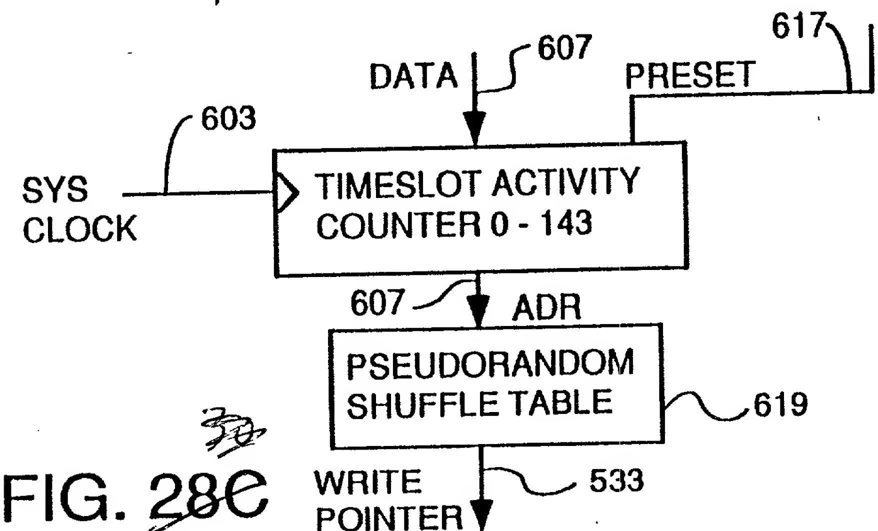


FIG. ~~28C~~ 40

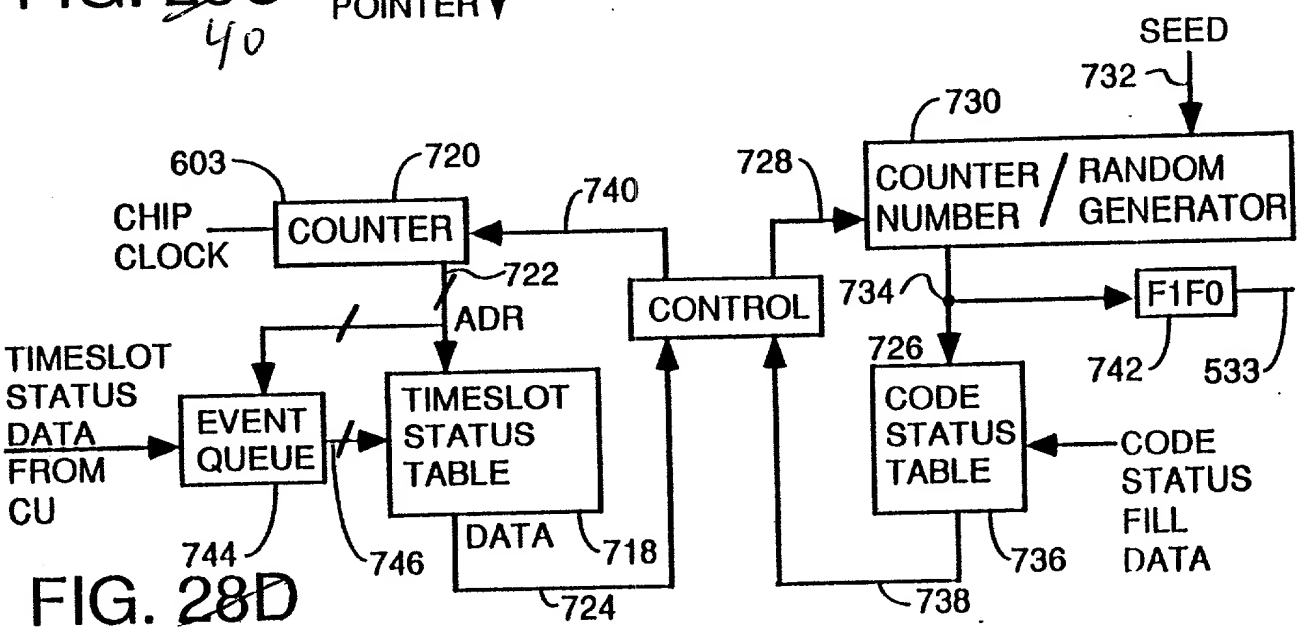


FIG. ~~28D~~ 41

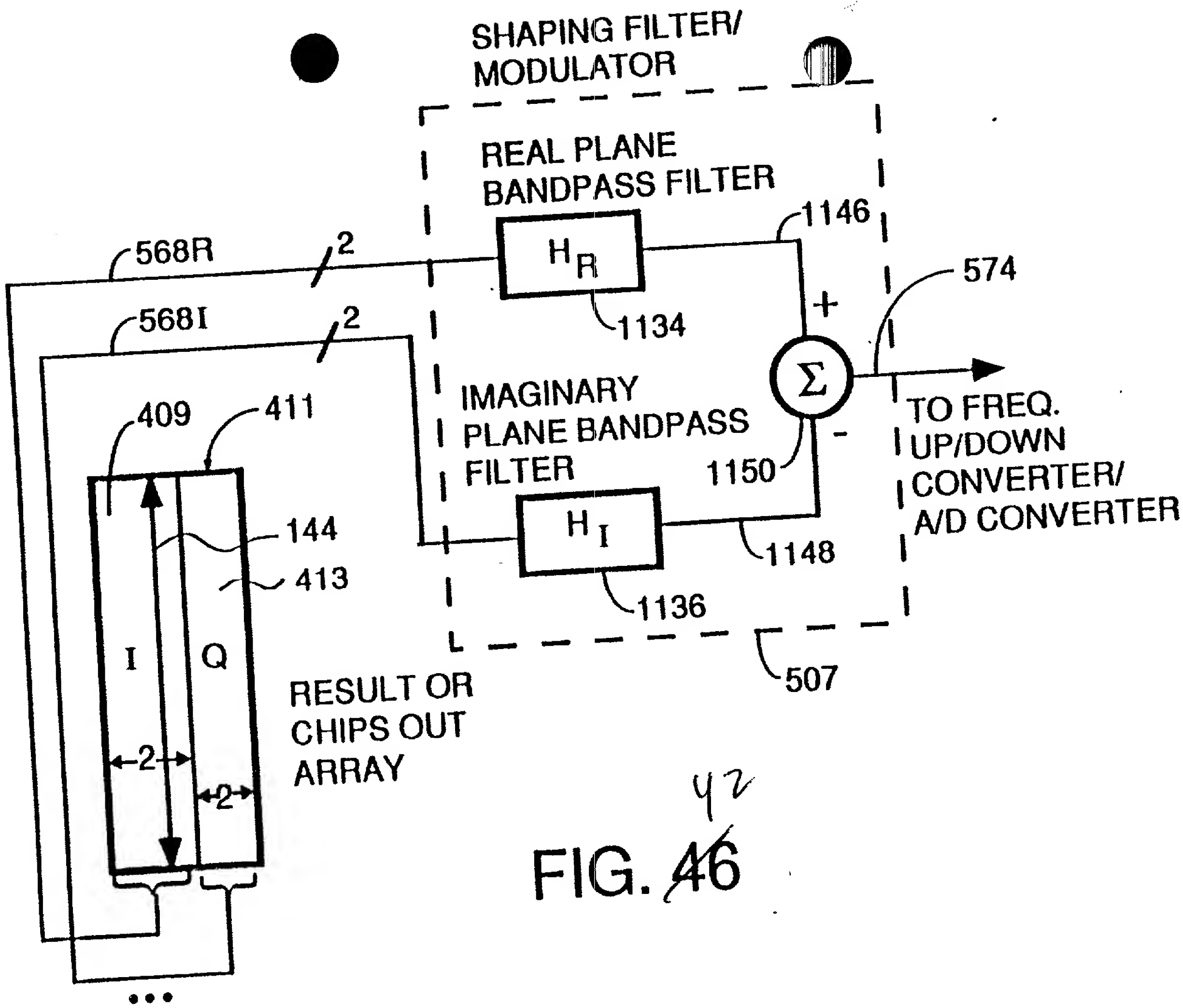


FIG. ~~46~~ 42

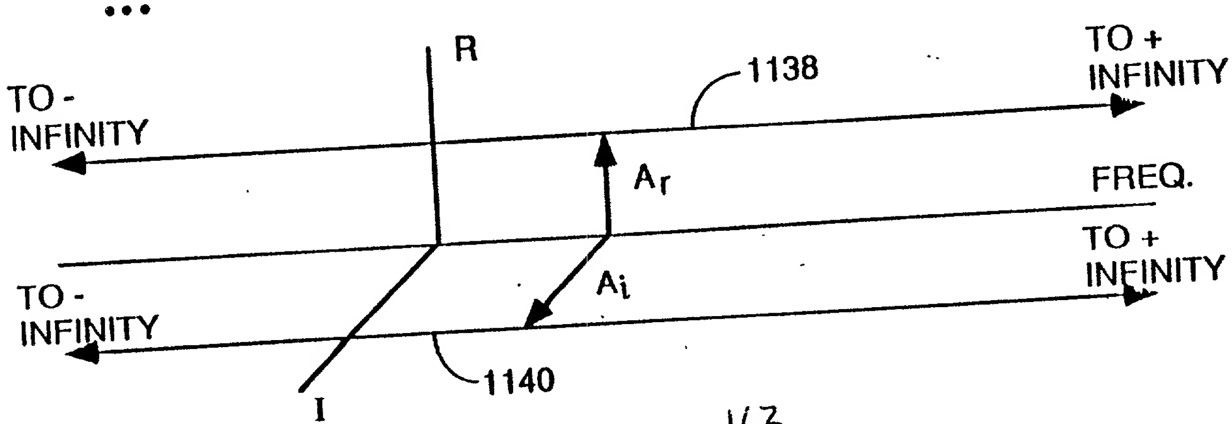


FIG. ~~47~~ 43

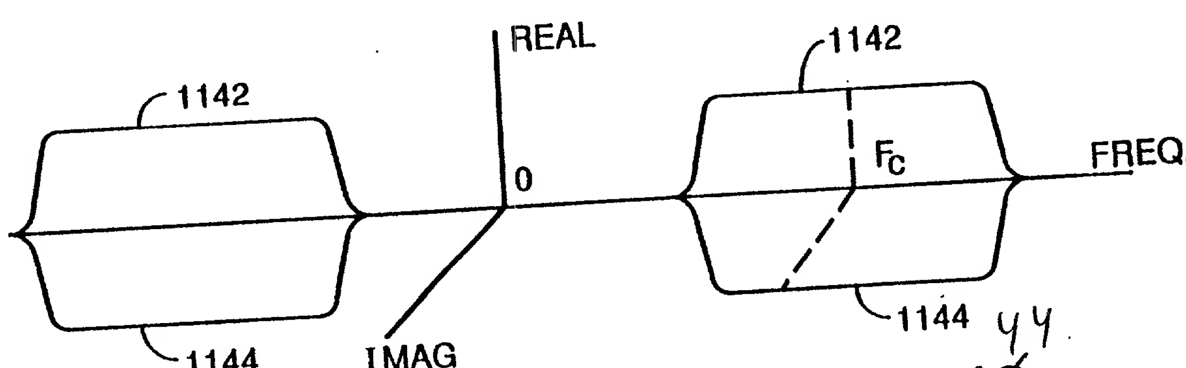
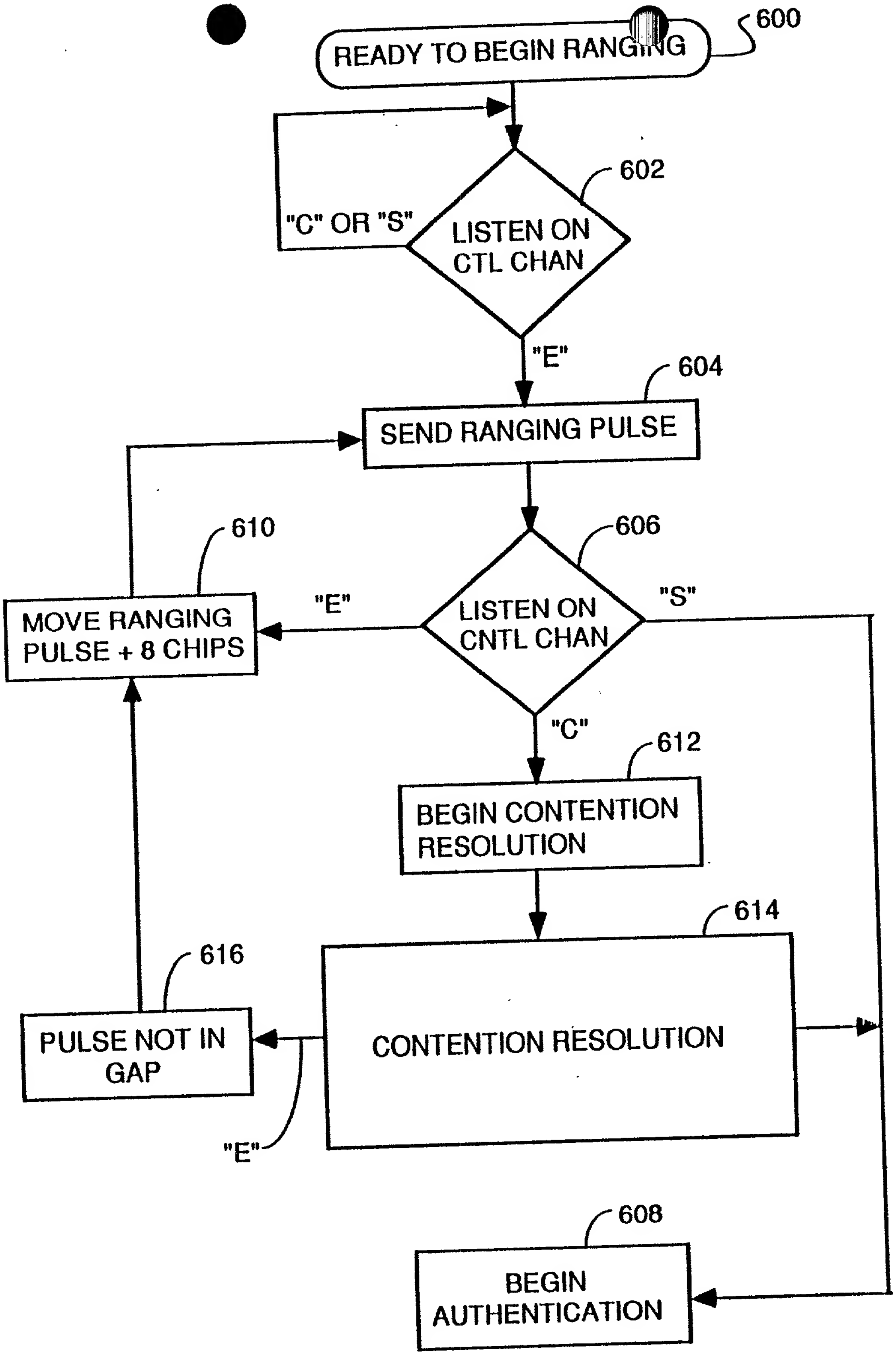
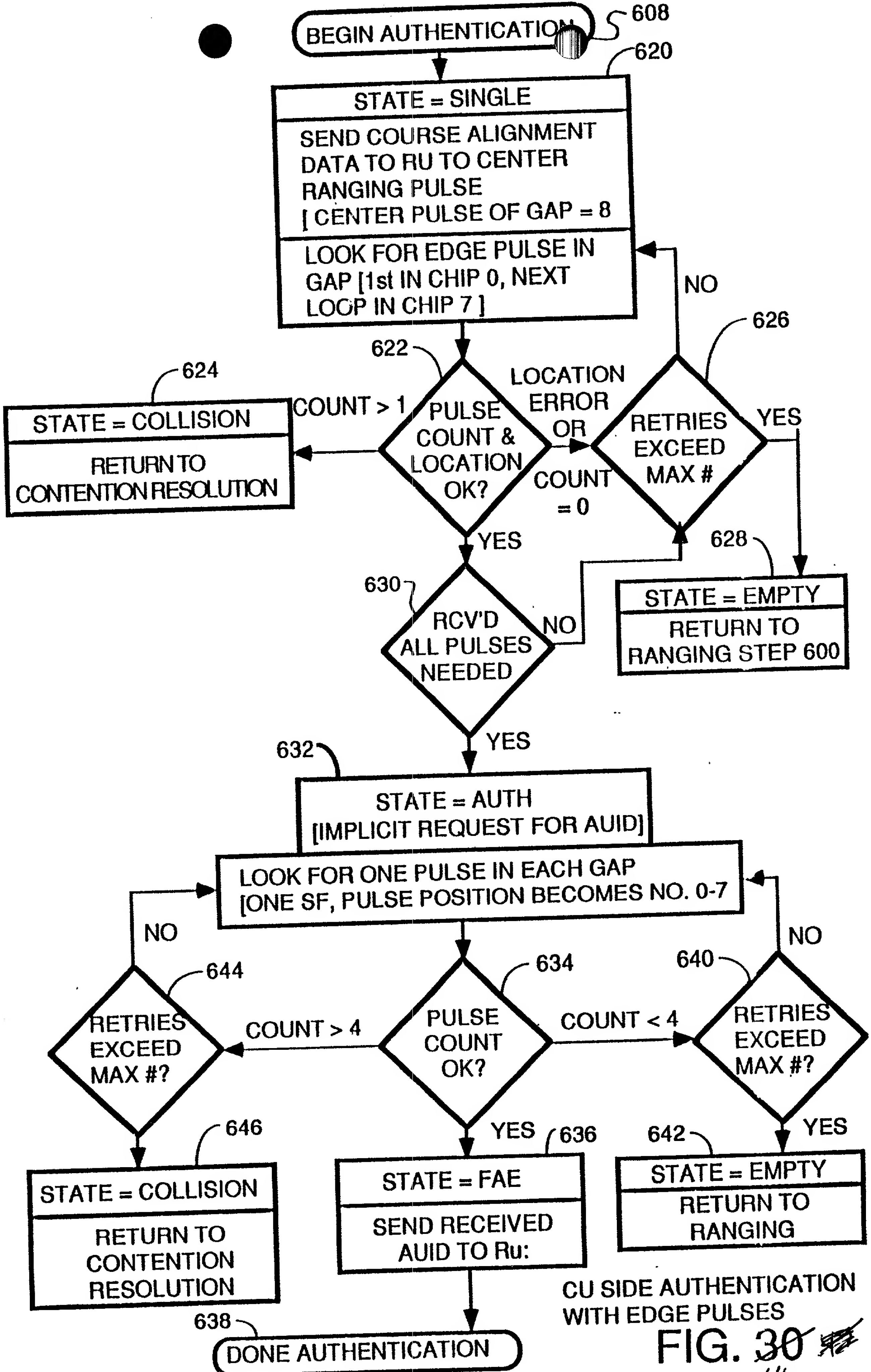


FIG. ~~48~~ 44



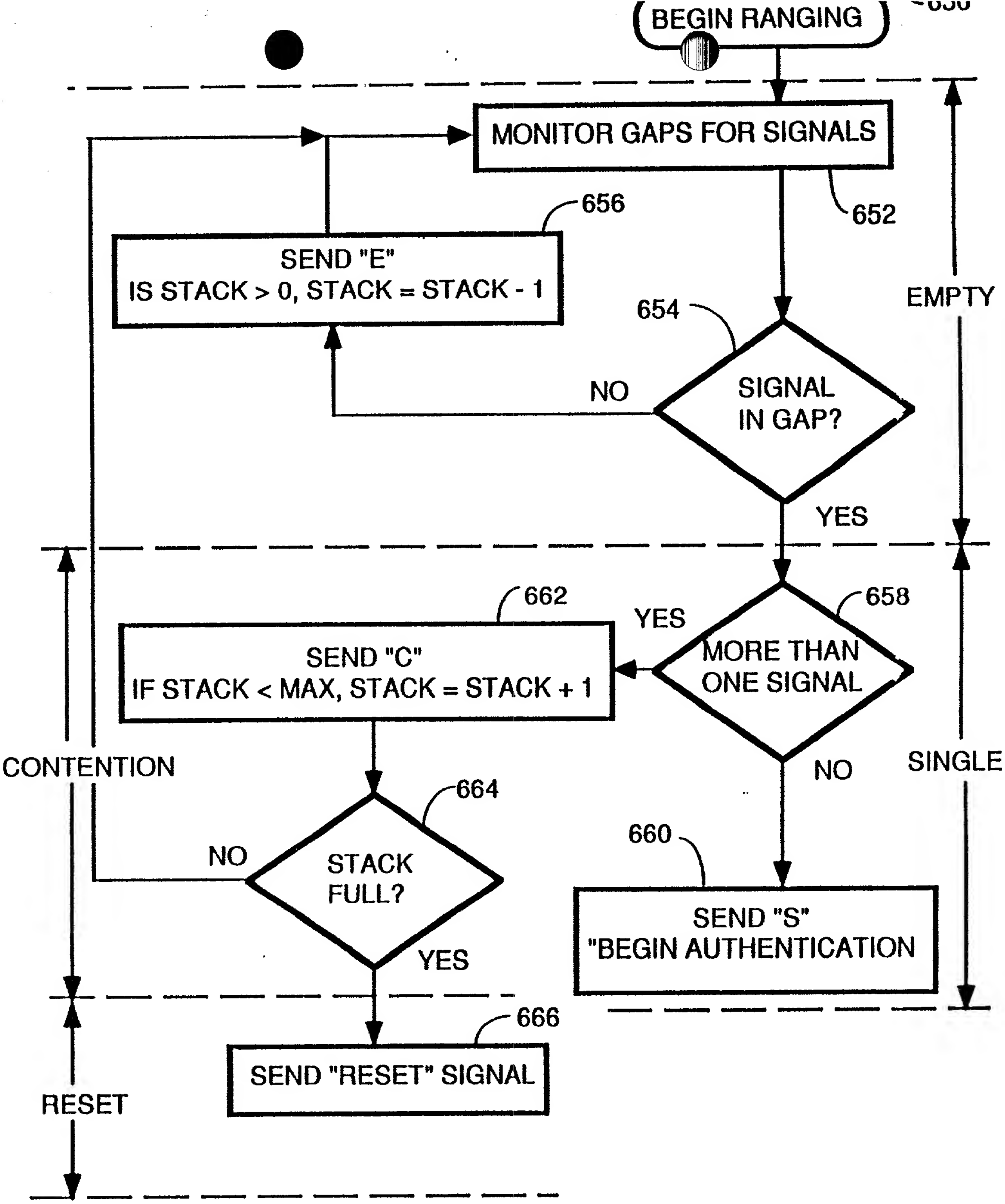
RU RANGING

FIG. 29



CU SIDE AUTHENTICATION WITH EDGE PULSES

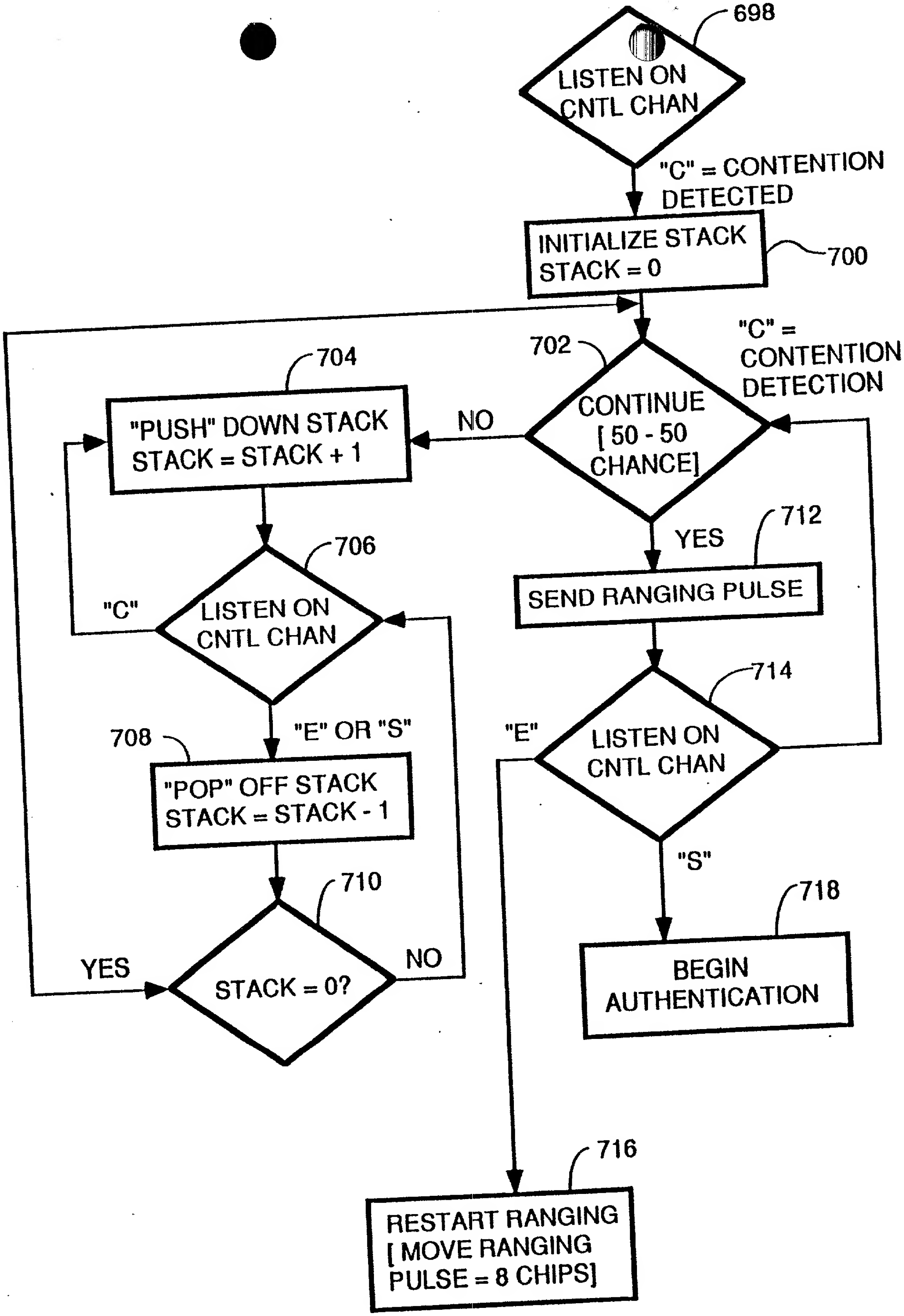
FIG. 30 46



CU RANGING & CONTENTION RESOLUTION

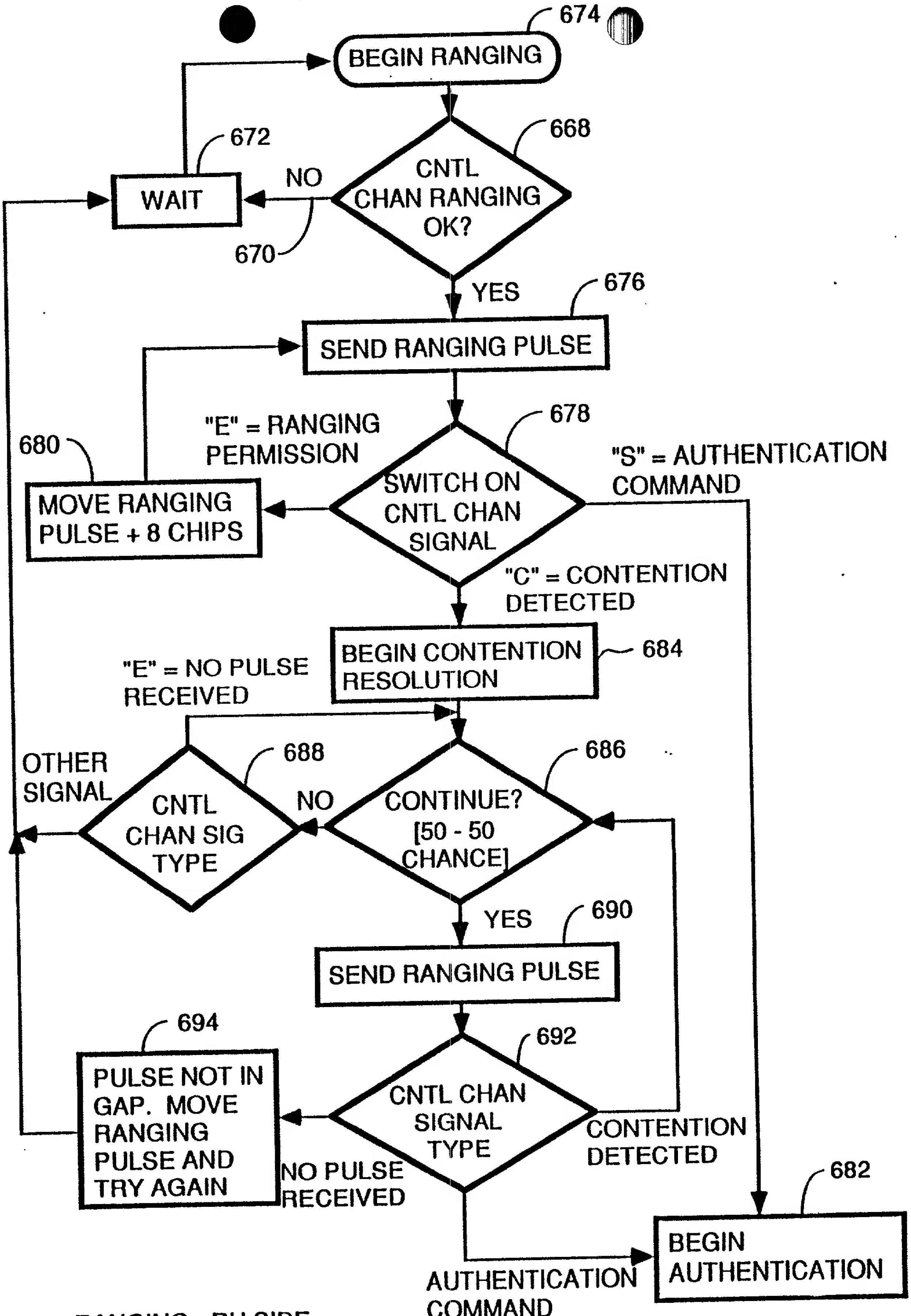
~~RANGING AND CONTENTION RESOLUTION~~
~~CU SIDE~~

FIG. ~~31~~ ~~48~~
47



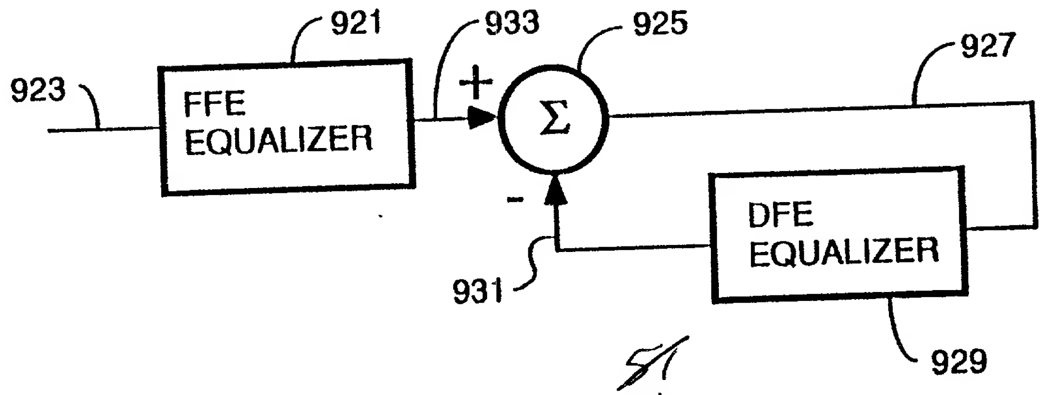
CONTENTION RESOLUTION - RU USING BINARY STACK

FIG. ~~33~~ 49

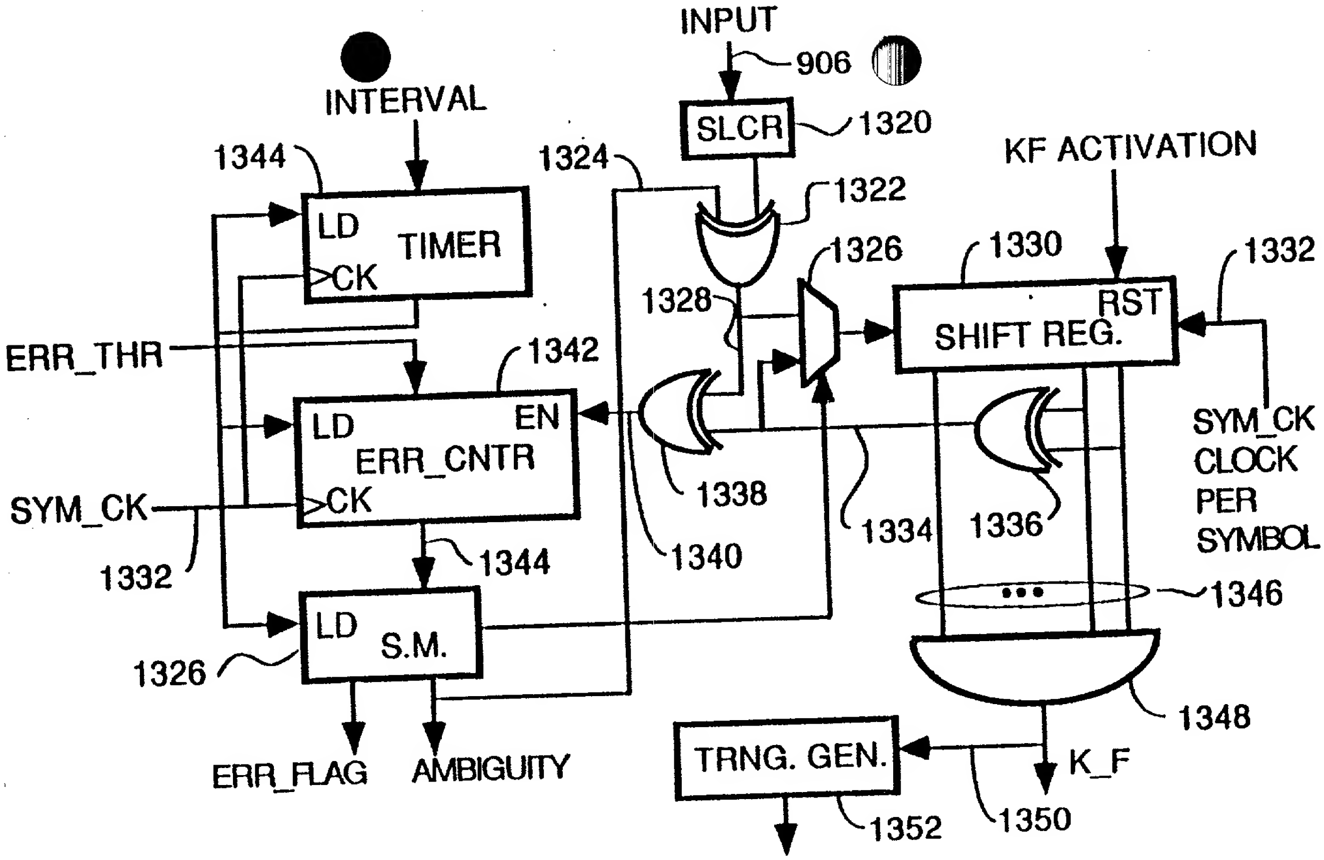


RANGING - RU SIDE
BINARY TREE
ALGORITHM

FIG. ~~32~~ ~~50~~ 49

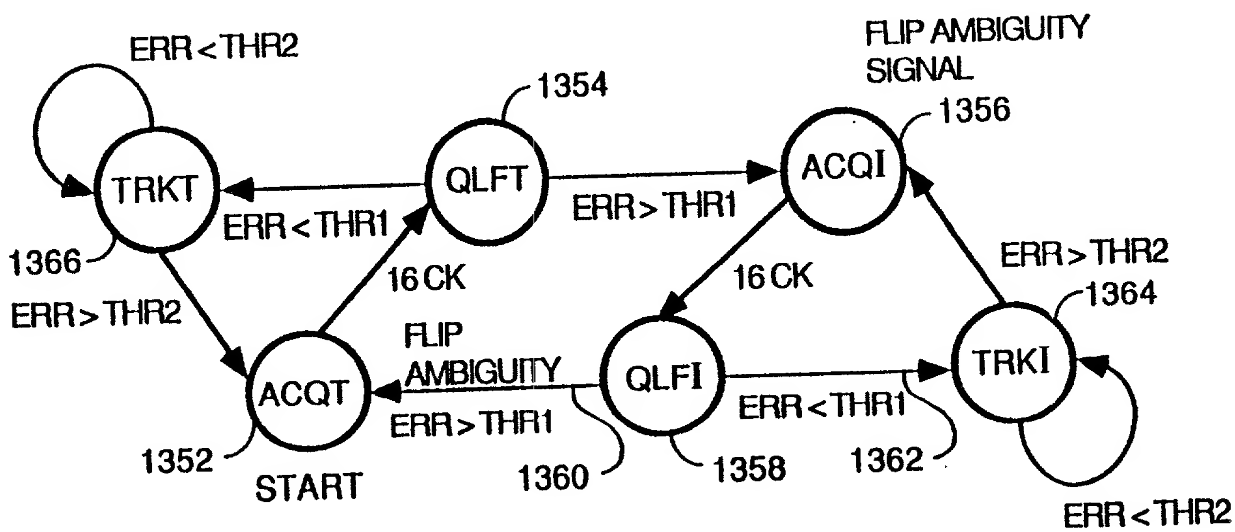


51
FIG. ~~37~~
50



FRAME DETECTOR
FRAME SYNC/KILOFRAME DETECT

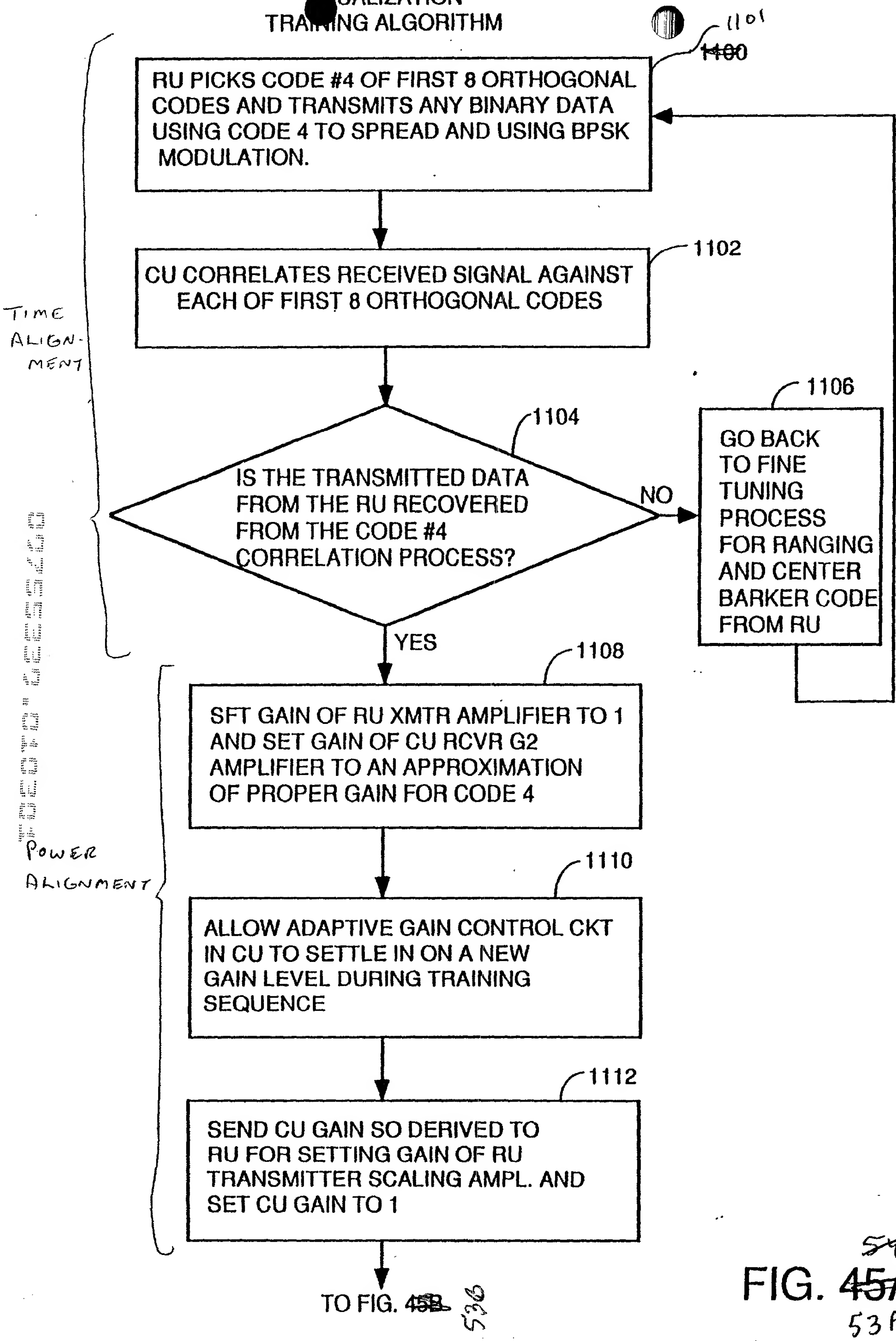
FIG. ~~52~~
51



STATE MACHINE

FIG. ~~53~~
52

PRECHANNEL
EQUALIZATION
TRAINING ALGORITHM



~~54A~~

FIG. ~~45A~~ 53A

UPSTREAM EQUALIZATION

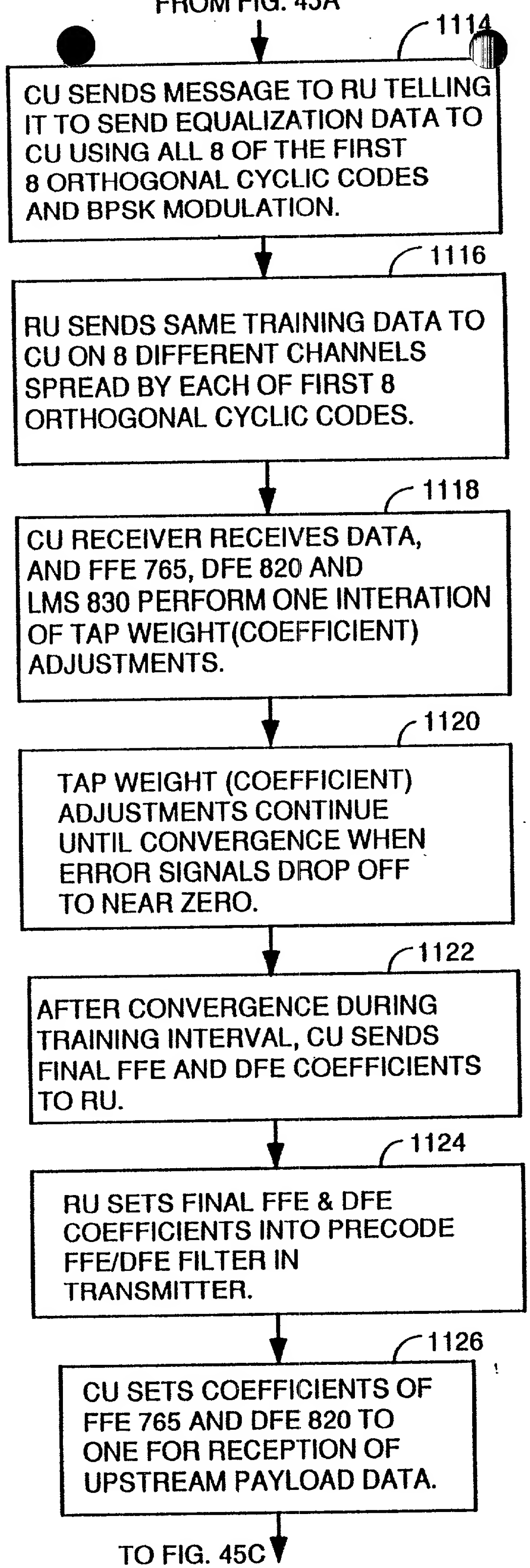


FIG. ~~45B~~ ~~54B~~ 53B

FROM FIG. 45B

DOWNSTREAM EQUALIZATION

1128

CU SENDS EQUALIZATION TRAINING DATA TO RU SIMULTANEOUSLY ON 8 CHANNELS SPREAD ON EACH CHANNEL BY ONE OF THE FIRST 8 ORTHOGONAL CYCLIC CODES MODULATED BY BPSK.

1130

RU RECEIVER RECEIVES EQUALIZATION TRAINING DATA IN MULTIPLE ITERATIONS AND USES LMS 830, FFE 765, DFE 820 AND DIFFERENCE CALCULATION CIRCUIT 832 TO CONVERGE ON PROPER FFE AND DFE TAP WEIGHT COEFFICIENTS.

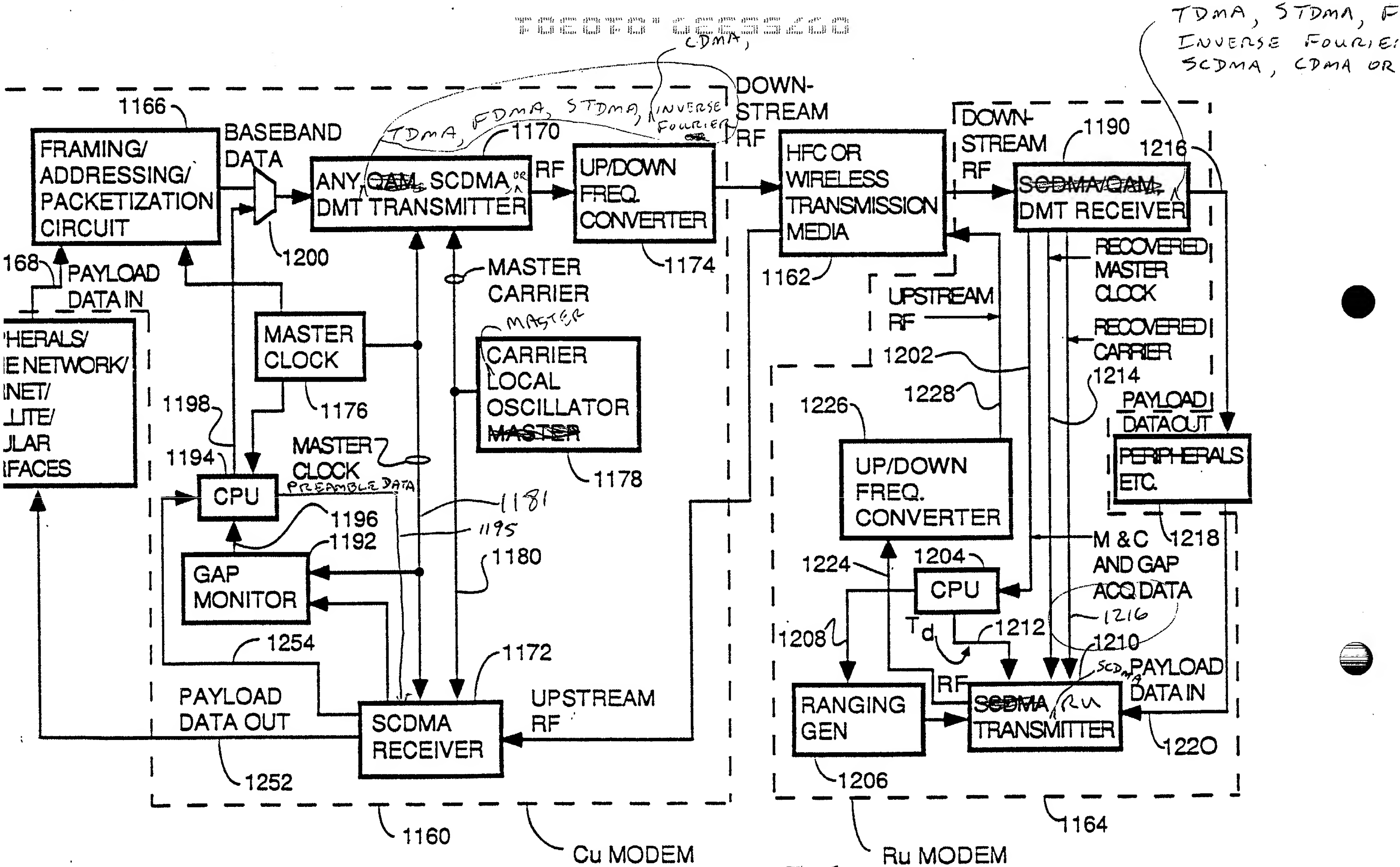
1132

AFTER CONVERGENCE, CPU READS FINAL TAP WEIGHT COEFFICIENTS FOR FFE 765 AND DFE 820 AND LOADS THESE TAP WEIGHT COEFFICIENTS INTO FFE/DFE CIRCUIT 764; CPU SETS FFE 765 AND DFE 820 COEFFICIENTS TO INITIALIZATION VALUES.

~~54C~~

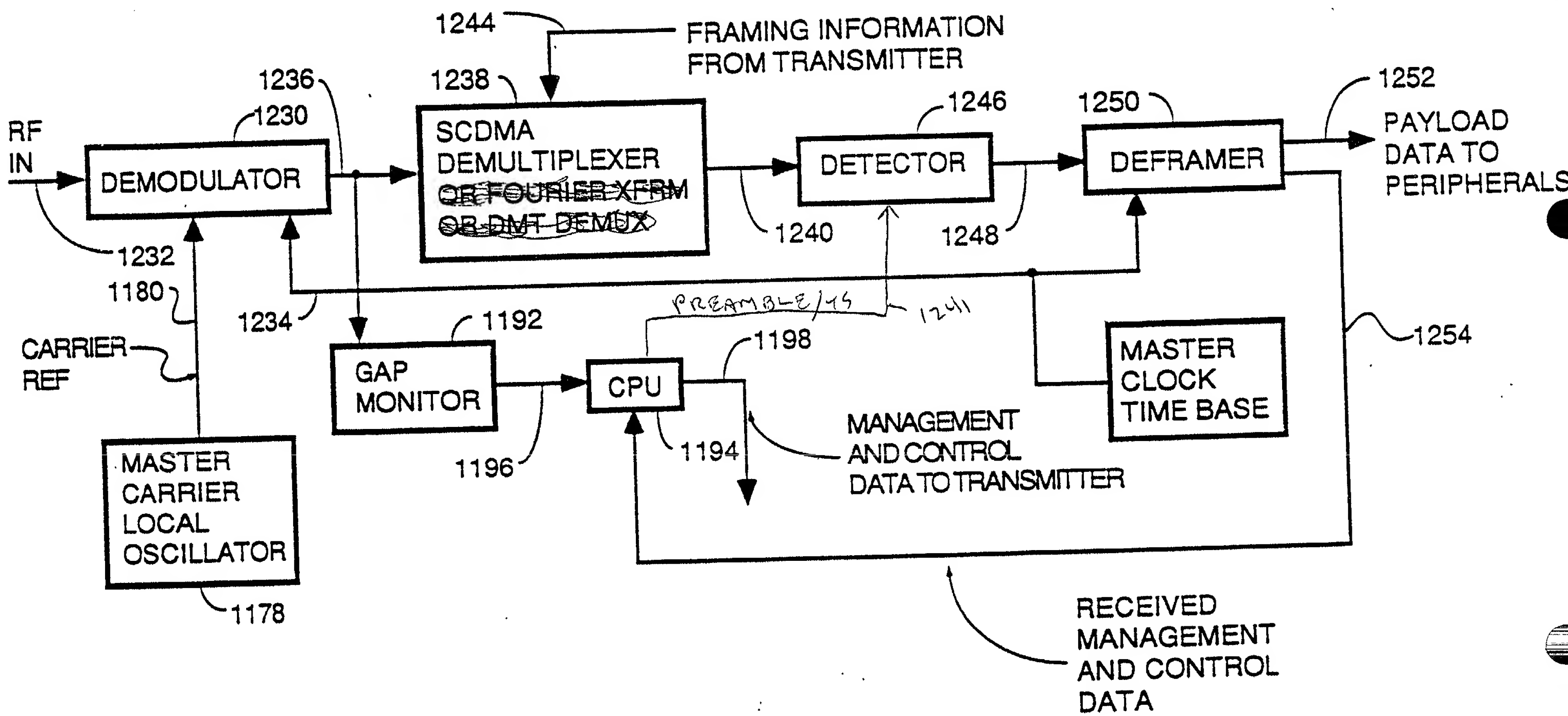
FIG. ~~45C~~

53C



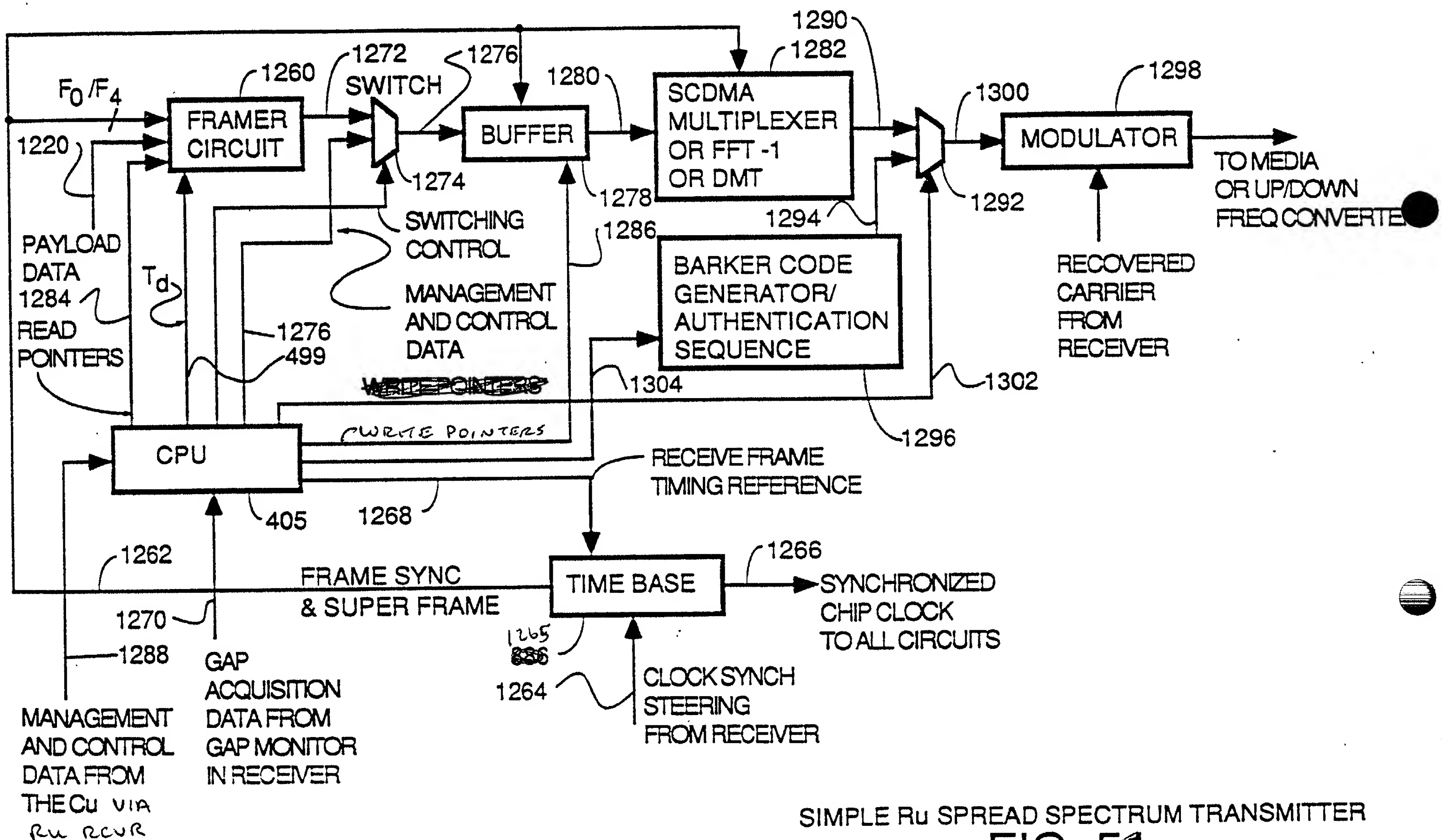
TDMA, STDMA, F
INVERSE FOURIER
SCDMA, CDMA OR
CDMA,
TDMA, FDMA, STDMA, INVERSE FOURIER
1166
FRAMING/ ADDRESSING/ PACKETIZATION CIRCUIT
BASEBAND DATA
1200
ANY ~~QAM~~ SCDMA OR DMT TRANSMITTER
1170
RF
UP/DOWN FREQ. CONVERTER
1174
DOWN-STREAM RF
HFC OR WIRELESS TRANSMISSION MEDIA
1162
DOWN-STREAM RF
1190
1216
~~SCDMA/QAM~~ DMT RECEIVER
RECOVERED MASTER CLOCK
RECOVERED CARRIER
1214
PAYLOAD DATA OUT
PERIPHERALS ETC.
1218
168
PAYLOAD DATA IN
HERALS/ E NETWORK/ NET/ LITE/ LAR FACES
MASTER CLOCK
1176
MASTER CARRIER
MASTER
CARRIER LOCAL OSCILLATOR ~~MASTER~~
1178
1198
1194
CPU
MASTER CLOCK
PREAMBLE DATA
1181
1195
1196
1192
1180
GAP MONITOR
1254
1172
PAYLOAD DATA OUT
SCDMA RECEIVER
UPSTREAM RF
1252
1160
Cu MODEM
UPSTREAM RF
1202
1228
1226
UP/DOWN FREQ. CONVERTER
1224
1204
CPU
M & C AND GAP ACQ DATA
1216
1210
1208
Td
1212
RF
SCDMA PAYLOAD DATA IN
RANGING GEN
~~SCDMA~~ RU TRANSMITTER
1220
1206
1164
Ru MODEM

FIG. ~~49~~ ~~53~~ 54



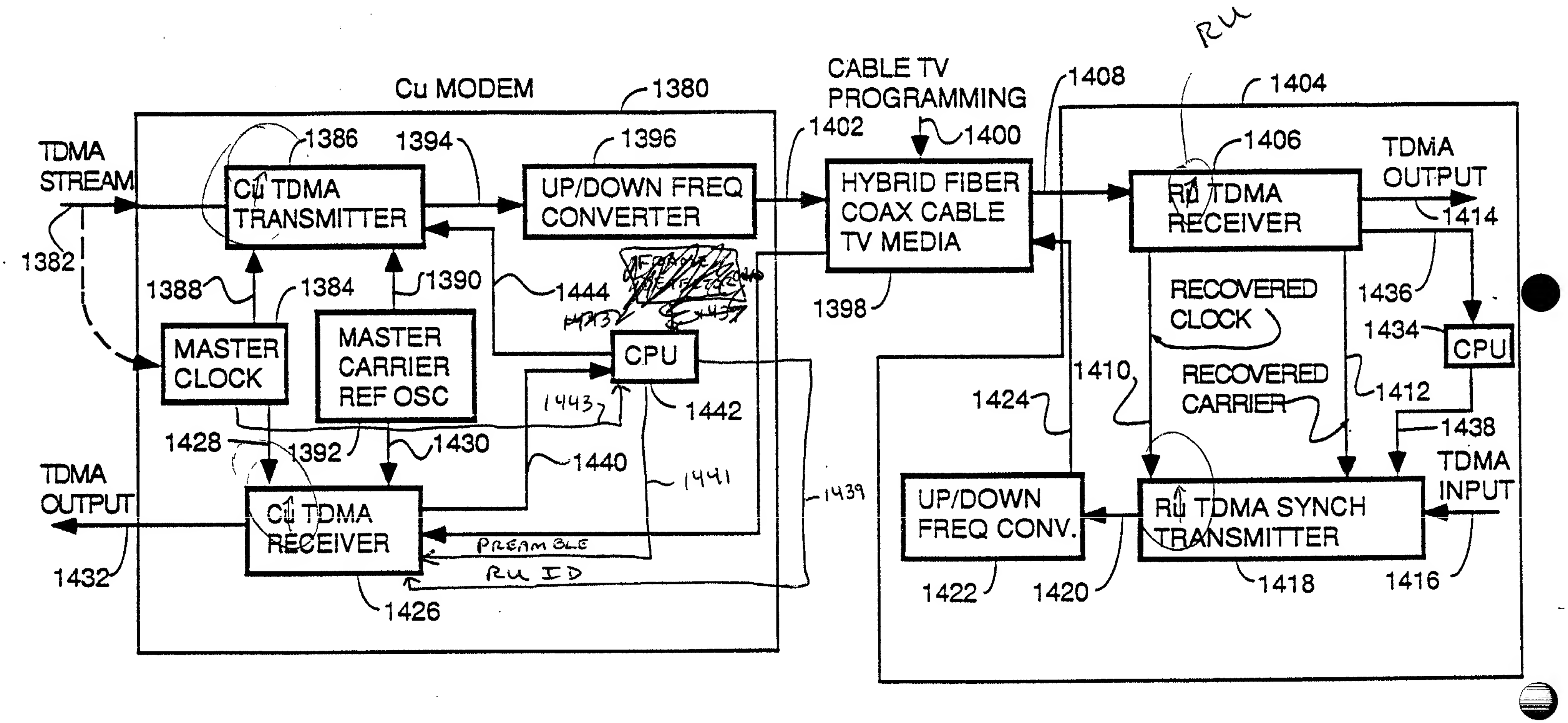
SIMPLE Cu SPREAD SPECTRUM RECEIVER

FIG. ~~50~~ ~~56~~ 55



SIMPLE Ru SPREAD SPECTRUM TRANSMITTER

FIG. ~~51~~ ~~57~~ 56



SYNCHRONOUS TDMA SYSTEM

FIG. ~~54~~ ~~58~~ 57

OFFSET (Chips)	1B ASIC RGSRH	1B ASIC RGSRL	2A ASIC RGSRH	2A ASIC RGSRL
0	0x0000	0x8000	0x0001	0x0000
1/2	0x0000	0xC000	0x0001	0x8000
1	0x0000	0x4000	0x0000	0x8000
-1	0x0001	0x0000	0x0002	0x0000

FIG. 58

Training Algorithm

SE Function

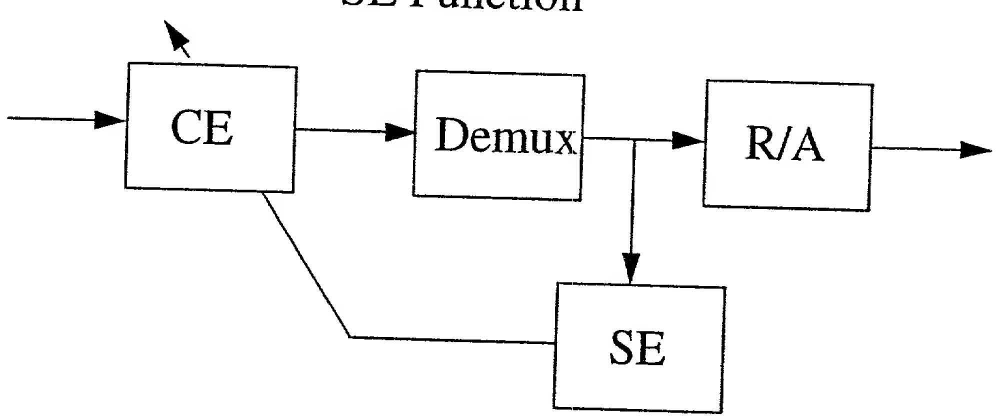
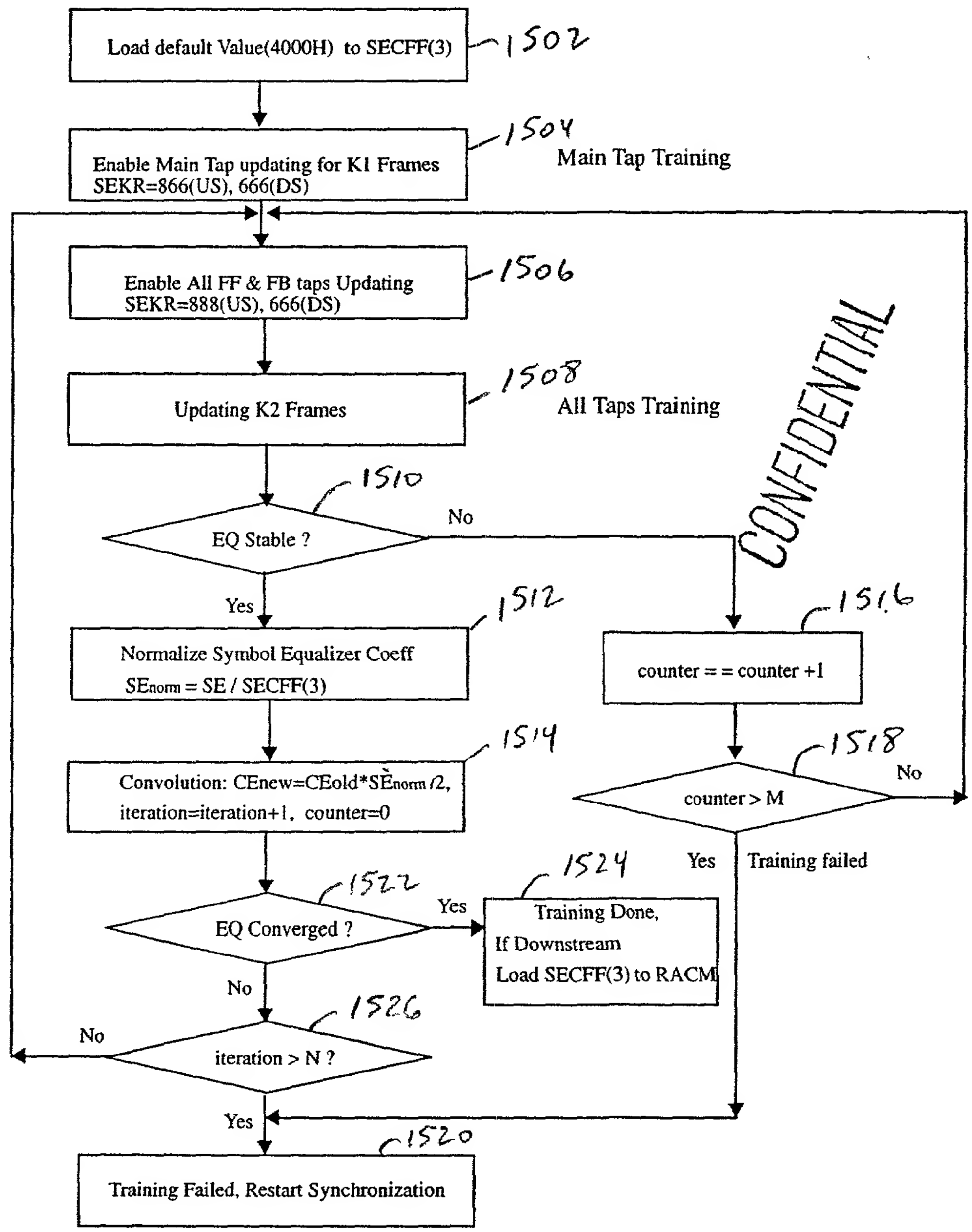


FIG. 59

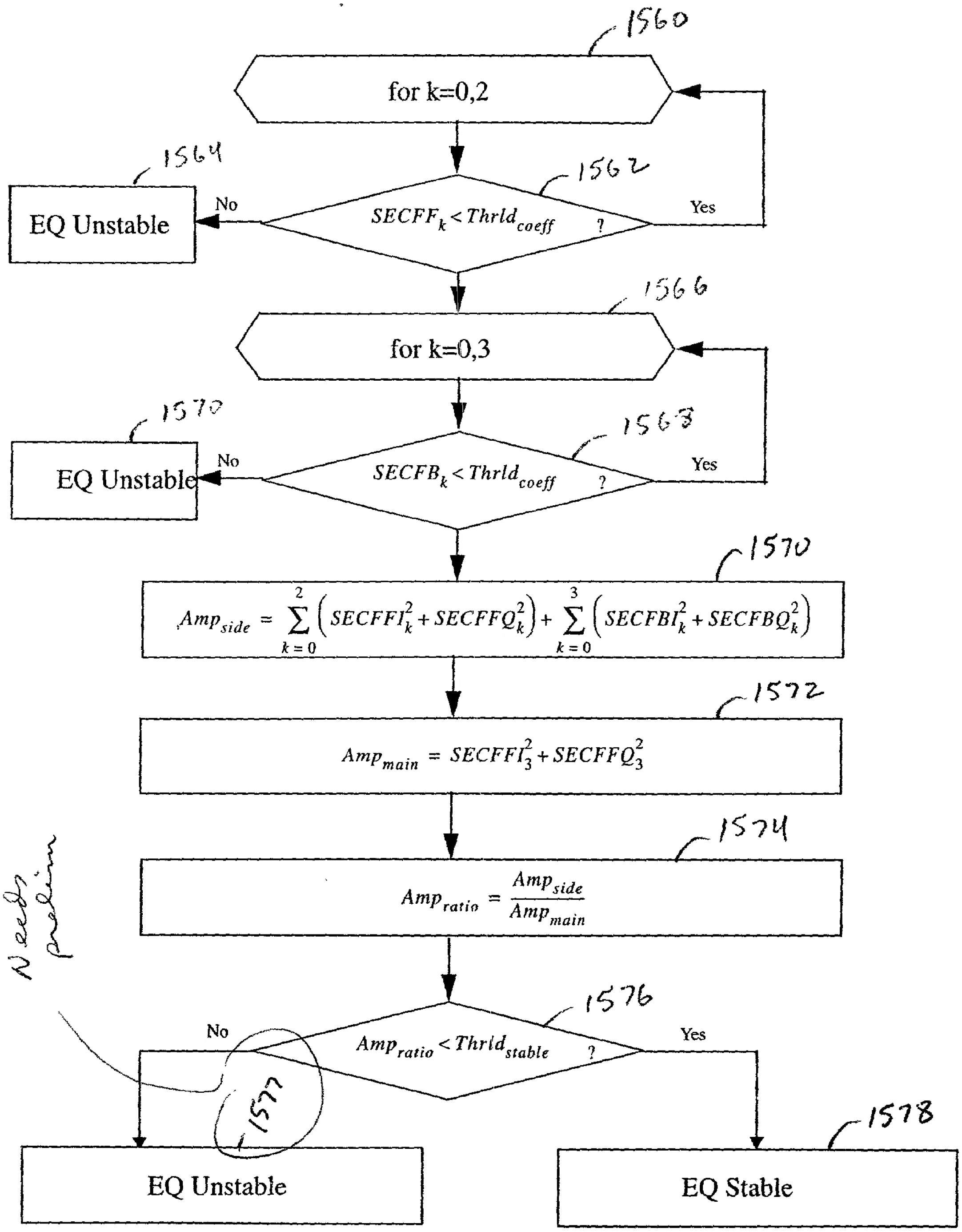
Initial 2-Step Training Algorithm



2-STEP INITIAL EQUALIZATION TRAINING

FIG. 60

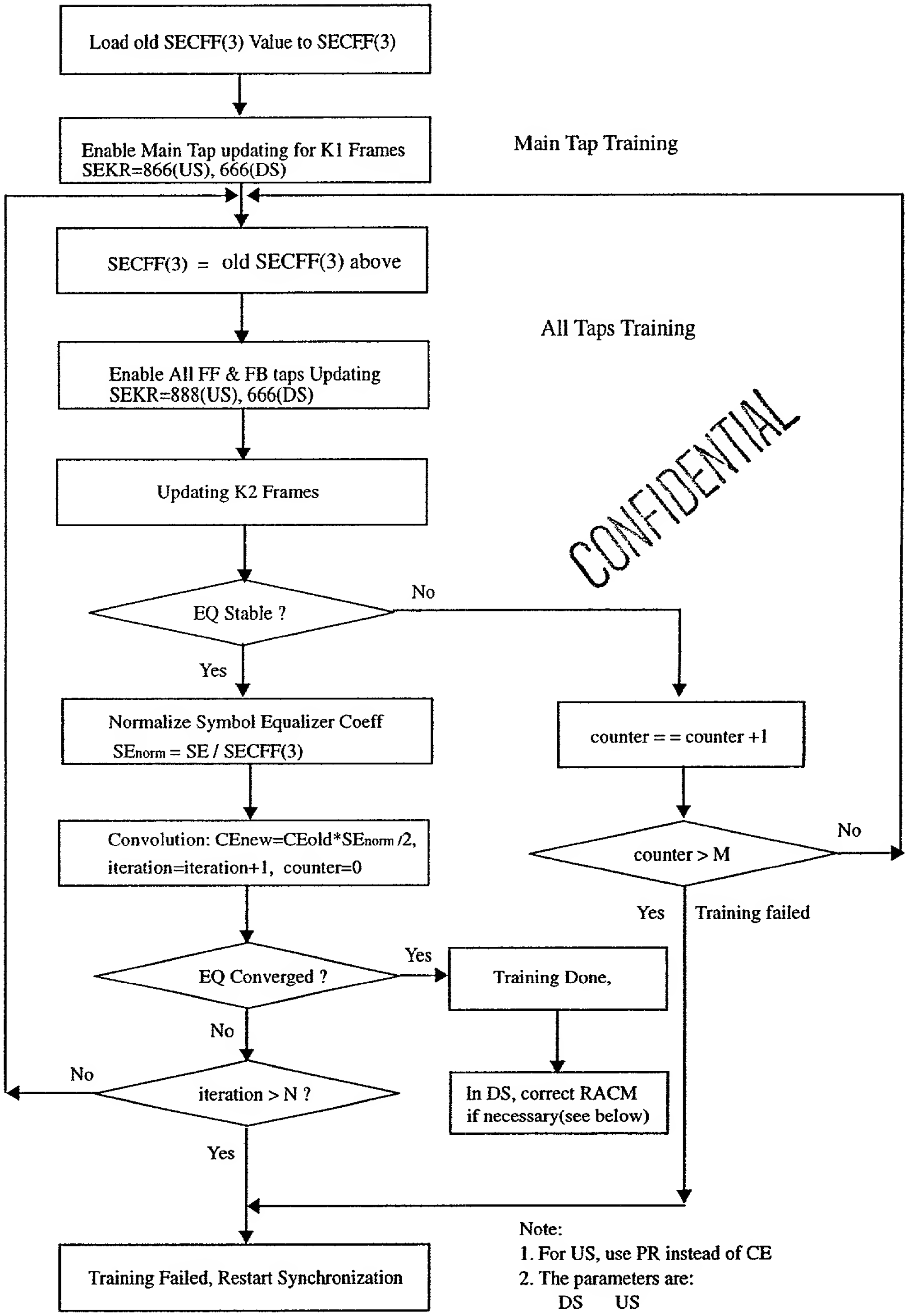
EQ Stability Check



Note: $Thrld_{coeff} = 7F00H$ $\quad Thrld_{stable} = 10^{-3}$

FIG. 61

Periodic 2-Step Training Algorithm

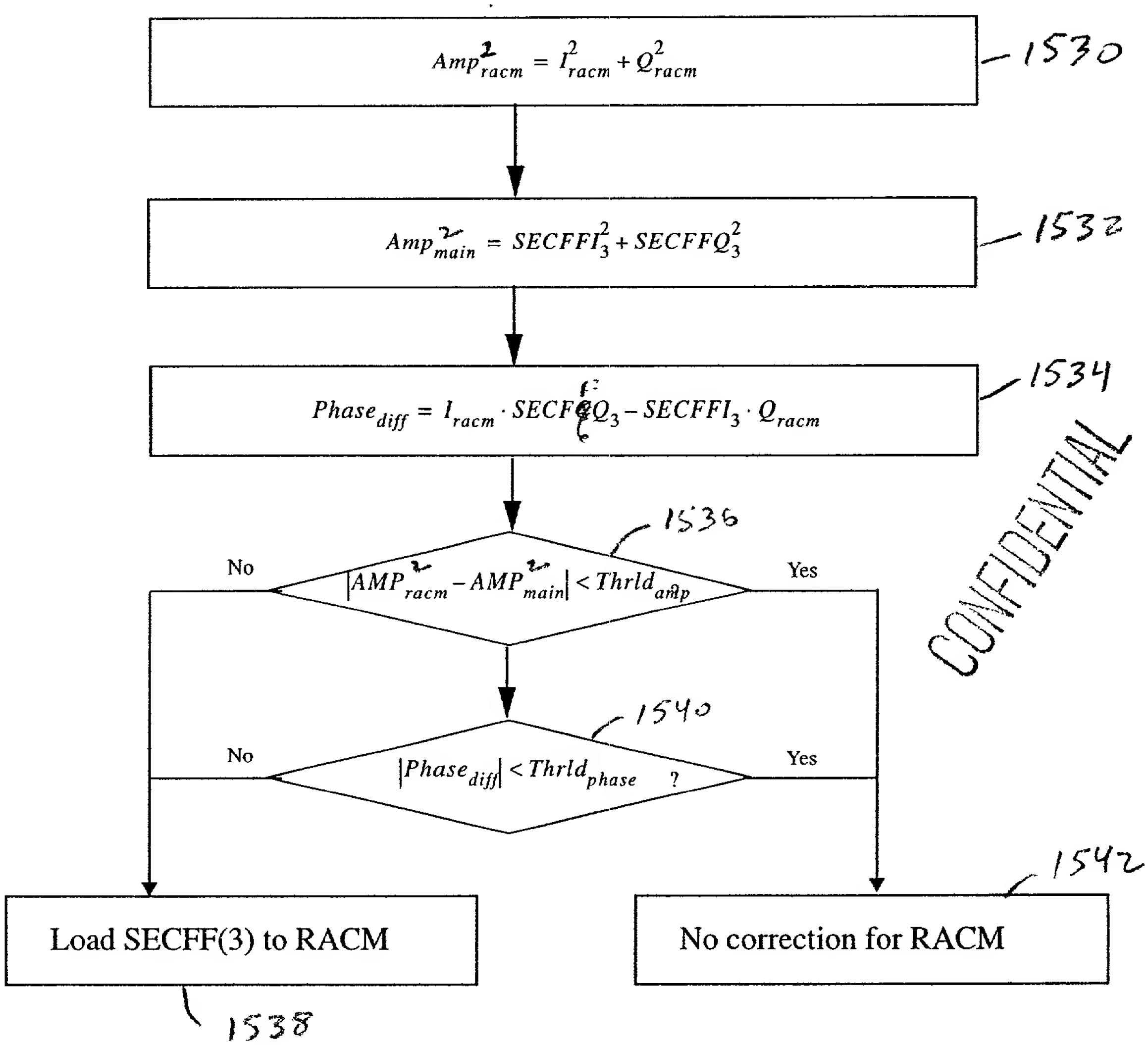


Note:
1. For US, use PR instead of CE
2. The parameters are:

	DS	US
K1	30	30
K2	20	30
N	5	3
M	3	3

FIG. 62

RACM Correction



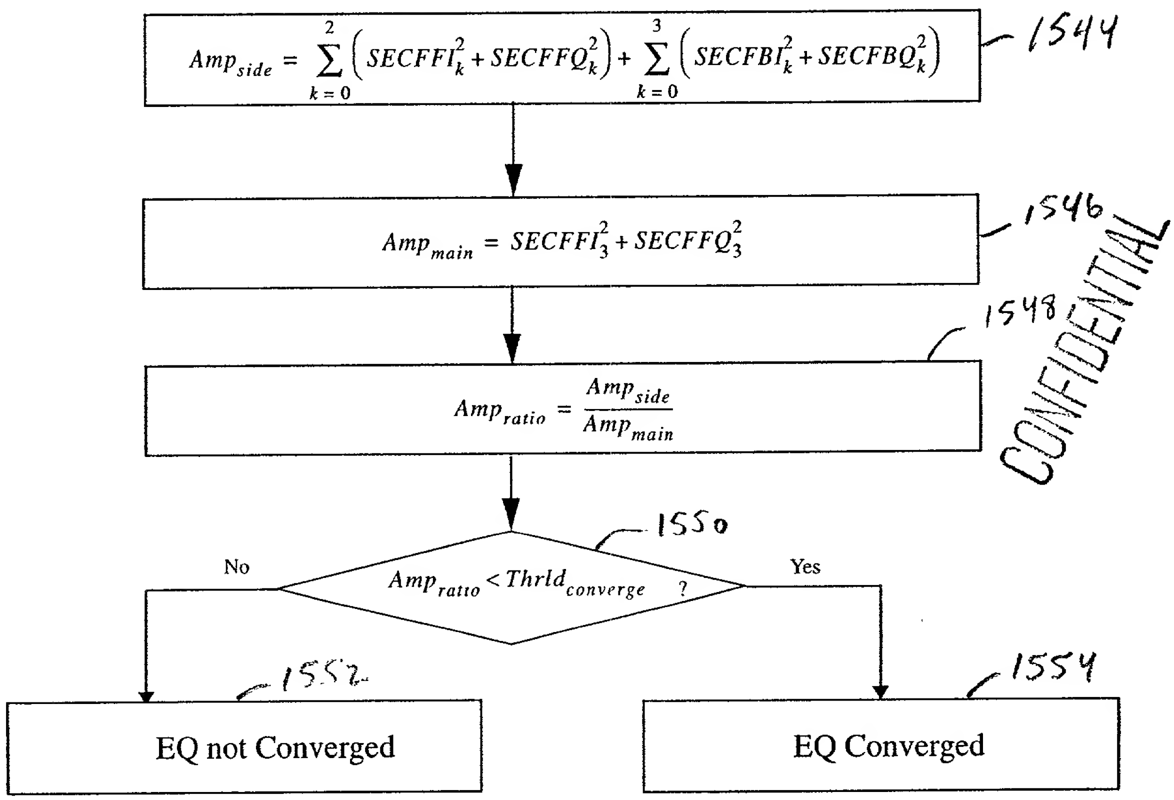
Note: $Thrld_{amp} = TBD$

$Thrld_{phase} = TBD$

ROTATIONAL AMPLIFIER CORRECTION

FIG. 63

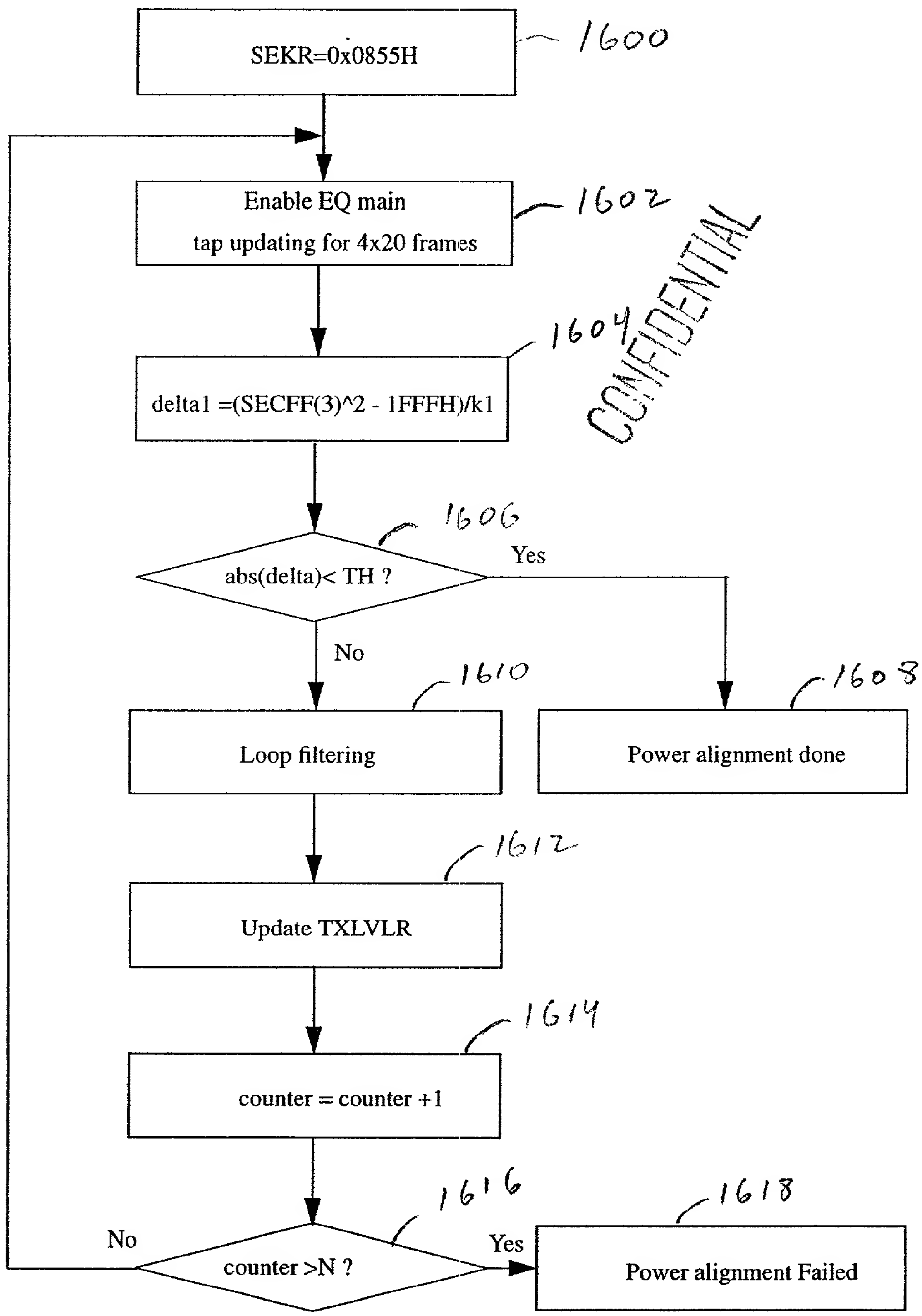
EQ Convergence Check



Note: $Thrld_{converge} = 10^{-5}$

FIG. 64

Power Alignment Flow Chart



Note: TH = 600H
N = 12

FIG. 65

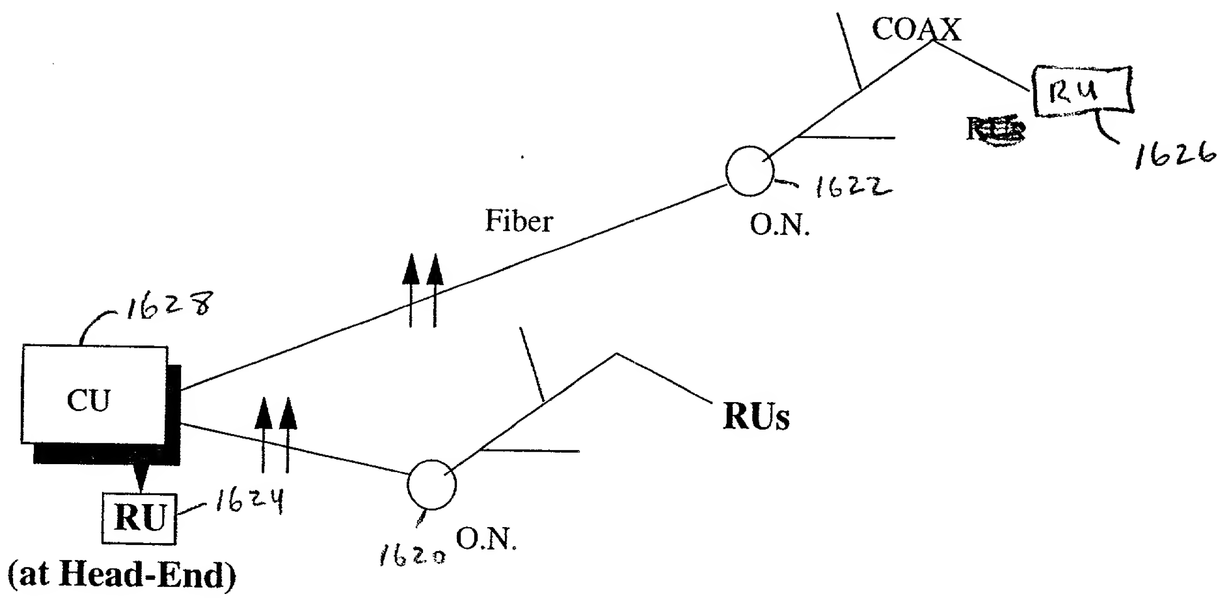

COAX
RU
1626
1622
Fiber
O.N.
1628
CU
RUs
RU
1624
(at Head-End)
1620
O.N.

FIG. 66

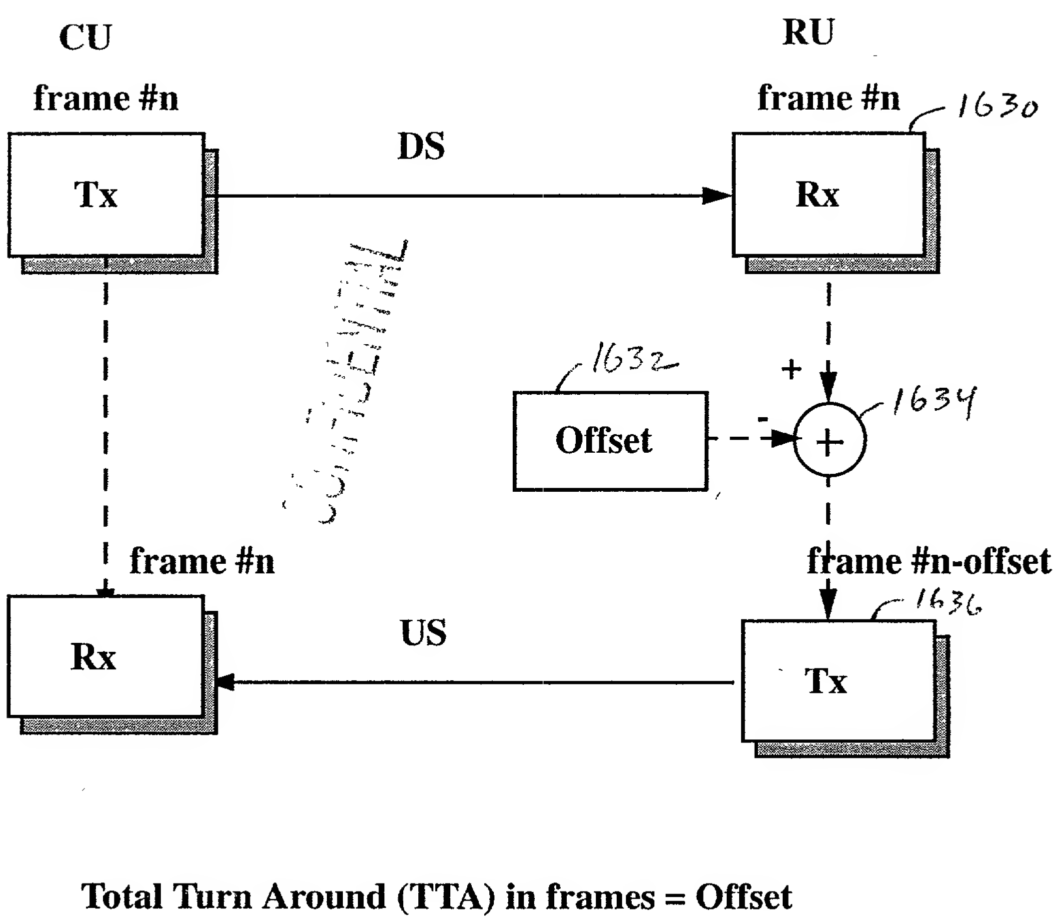

CU
frame #n
RU
frame #n
1630
Tx
DS
Rx
1632
+
1634
Offset
-
+
frame #n
frame #n-offset
1636
Rx
US
Tx
Total Turn Around (TTA) in frames = Offset

FIG. 67

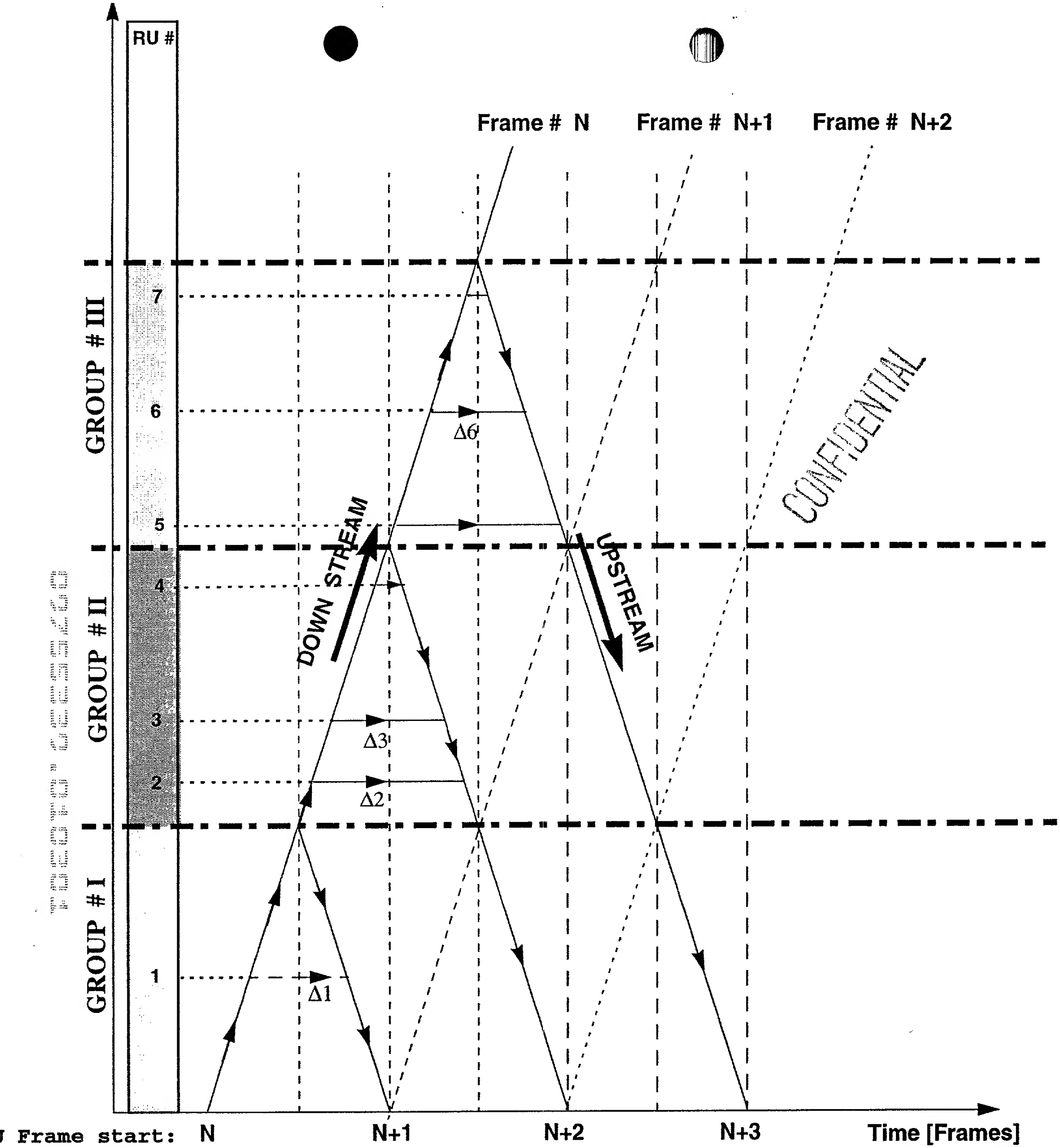


FIG. 68

~~Figure 3.1: Frame start propagation along the channel~~

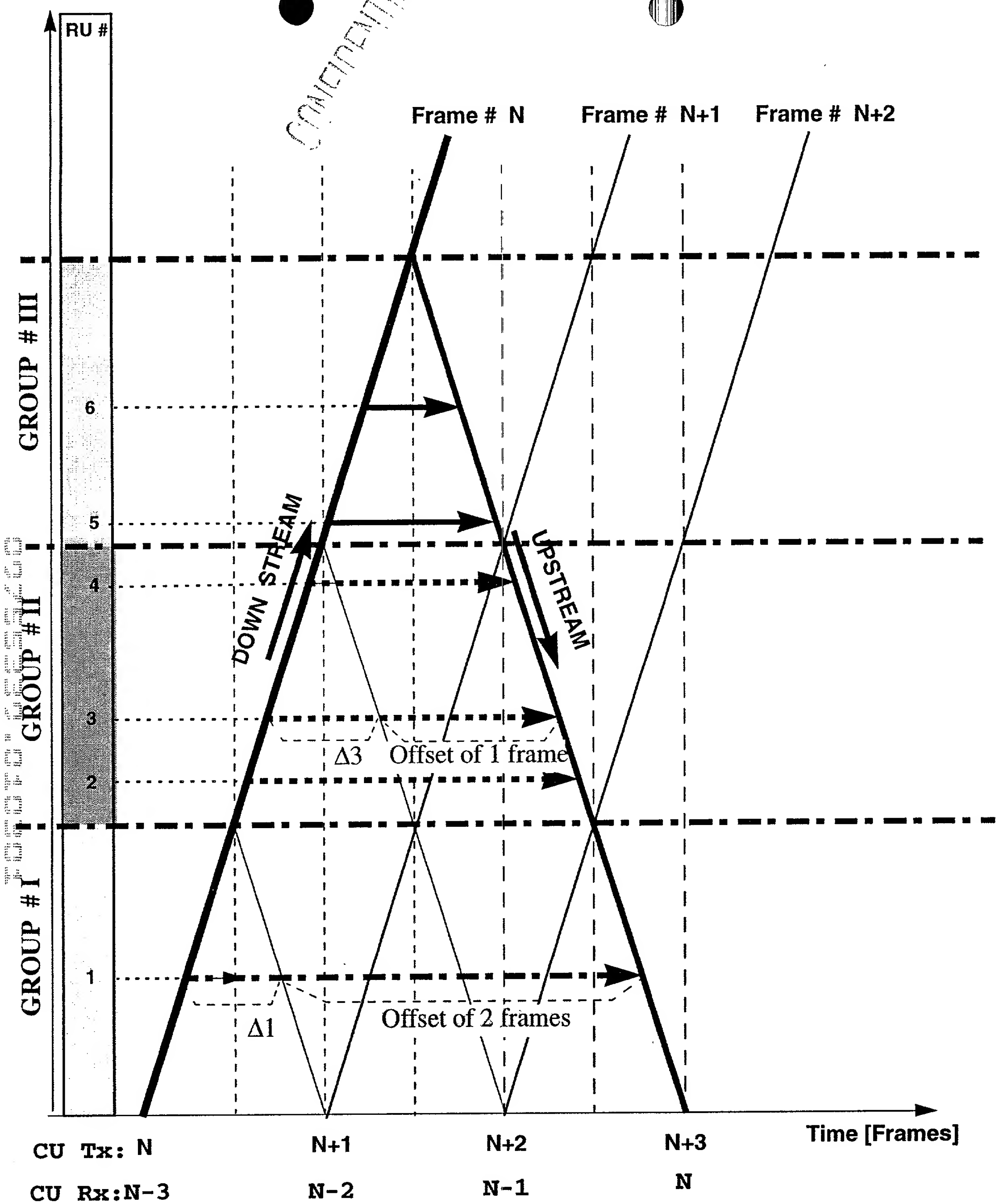


FIG. 69

[redacted] Control message (downstream) and function (upstream) propagation in a 3 frames TTA channel

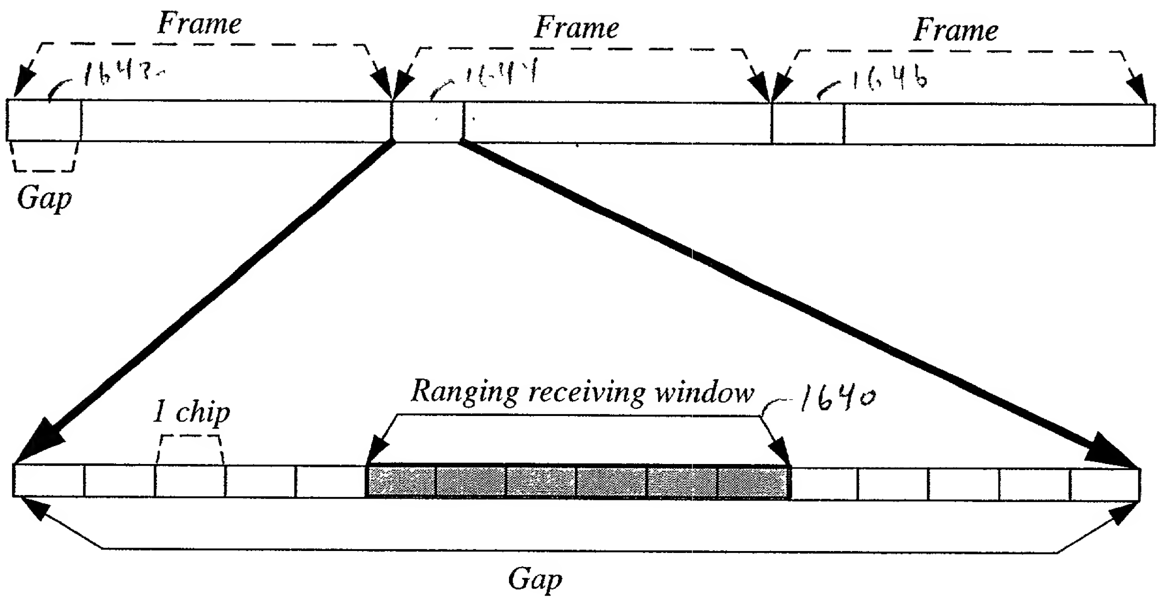
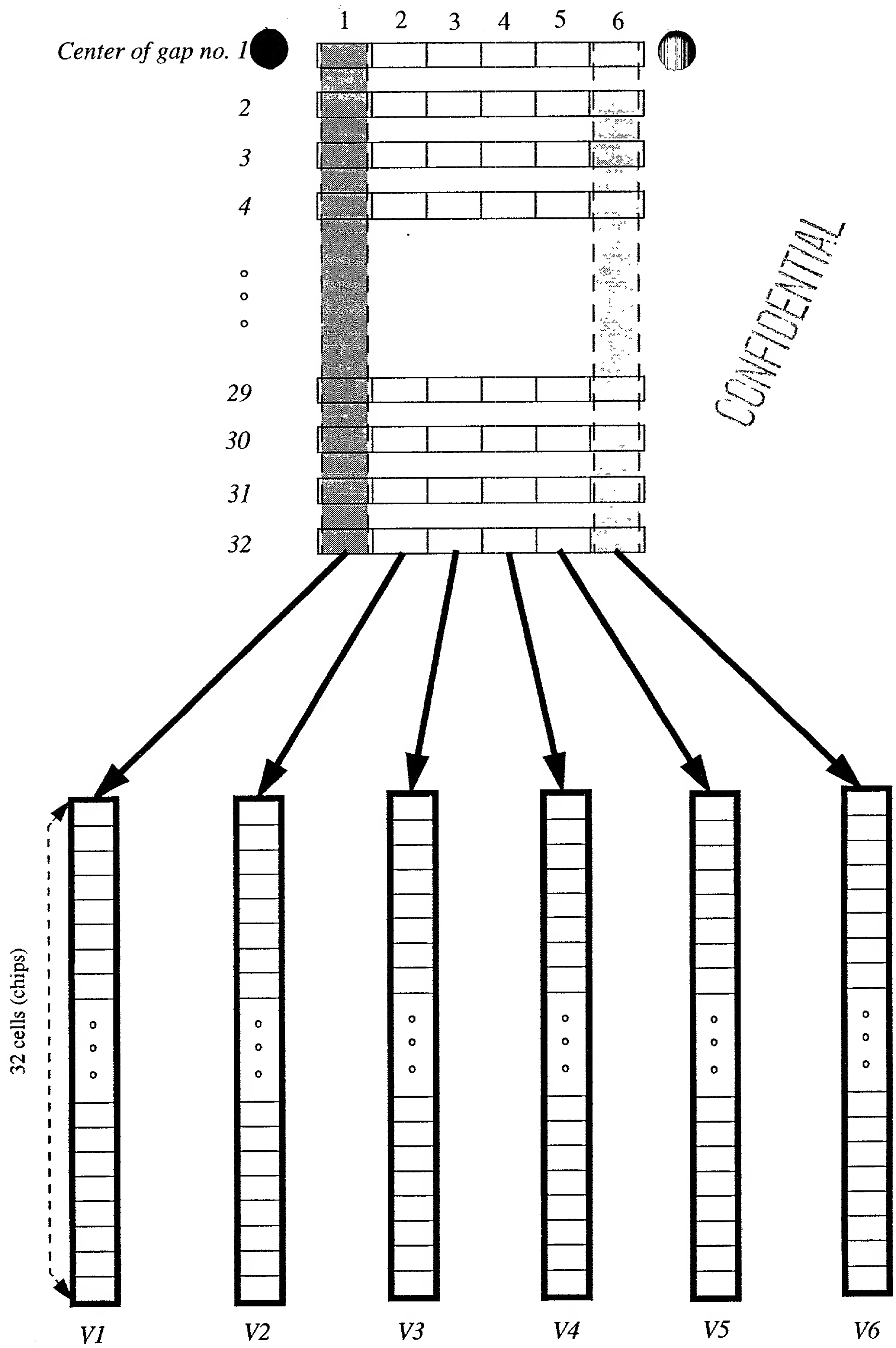

Frame
Frame
Frame
1642
1644
1646
Gap
Ranging receiving window
1640
1 chip
Gap

FIG. 70



~~Figure 3.4:~~ **Overall view of the CU sensing windows in a "boundless ranging" algorithm**

FIG. 71

6

Chip\FR	1	2	3	4	5	6	7		33
1	0	0	1	0	0	1	1	...	0
2	1	0	0	1	1	1	1	...	
3	0	0	0	1	1	1			
4	0	0	0	1	0	0	0	...	0
5	0	1	0	0	1				
6	0	0	1	1	1				
7	0	0	0	1	1				
8	0	0	0	0	1	0	0	...	

FIG. 72